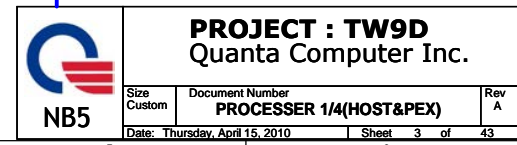
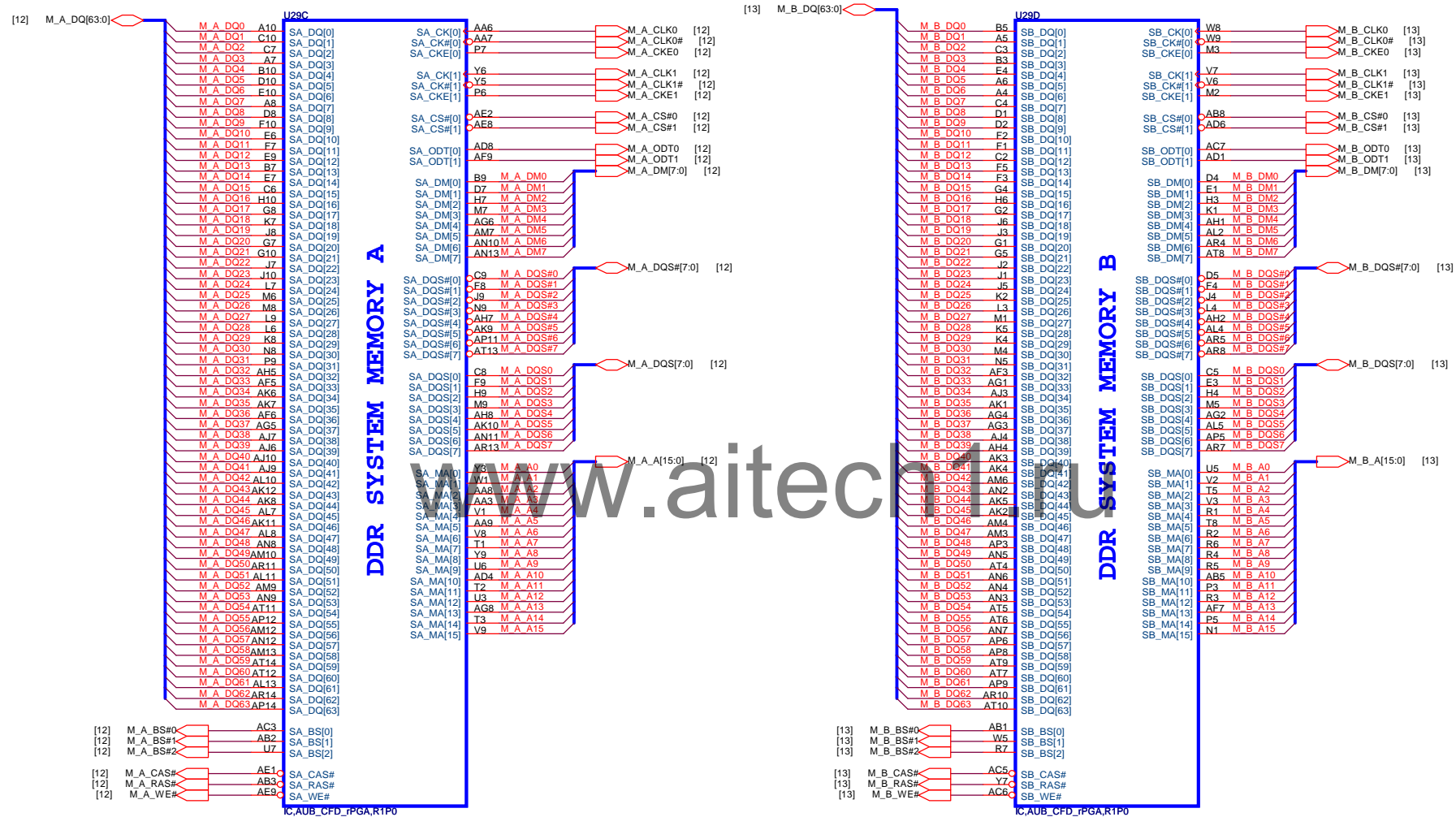
 NB5	PROJECT : TW9D Quanta Computer Inc.		
	Size Custom	Document Number Block Diagram	Rev A
Date: Thursday, April 15, 2010		Sheet 1 of 43	

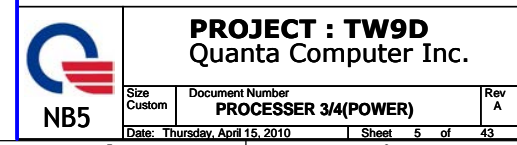


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



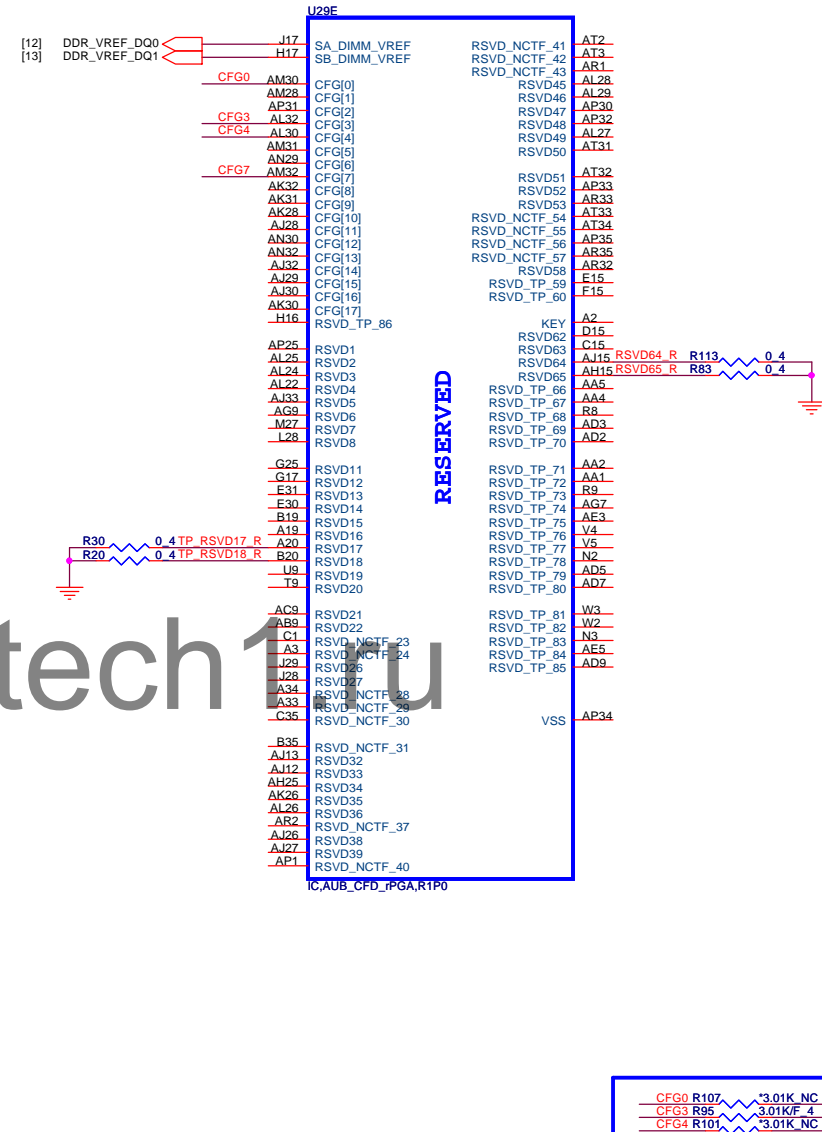
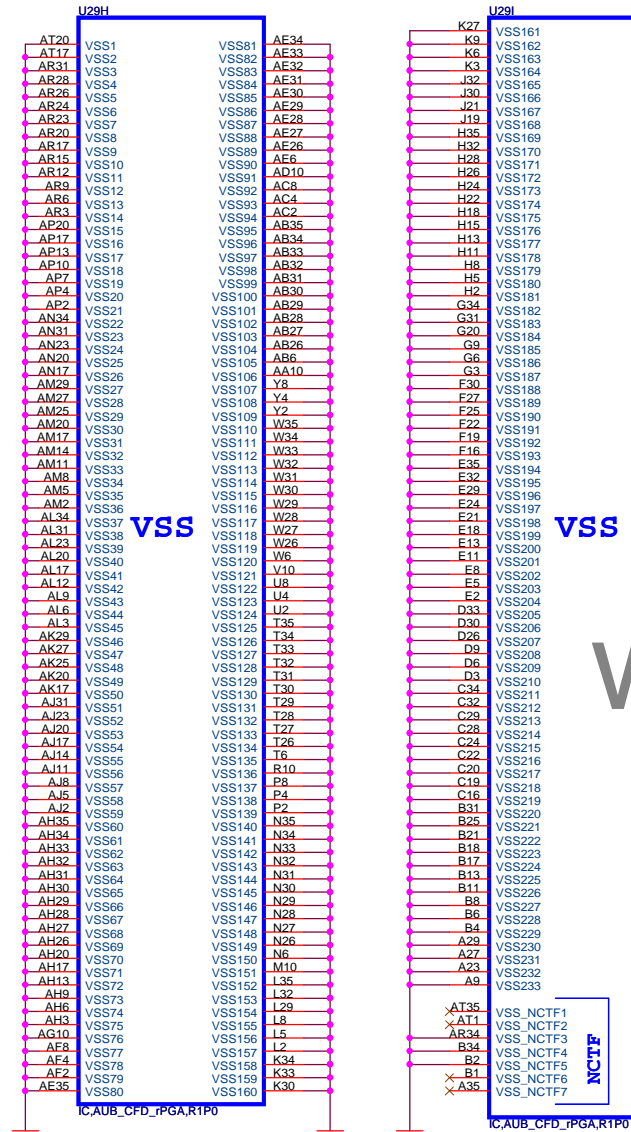
PROJECT : TW9D
Quanta Computer Inc.

Size Custom	Document Number PROCESSOR 2/4(DDR)	Rev A
Date: Thursday, April 15, 2010		Sheet 4 of 43

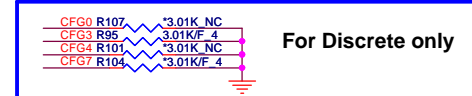


AUBURNDAL/CLARKSFIELD PROCESSOR (GND)

AUBURNDAL/CLARKSFIELD PROCESSOR(RESERVED, CFG)



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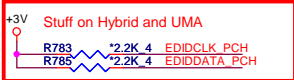
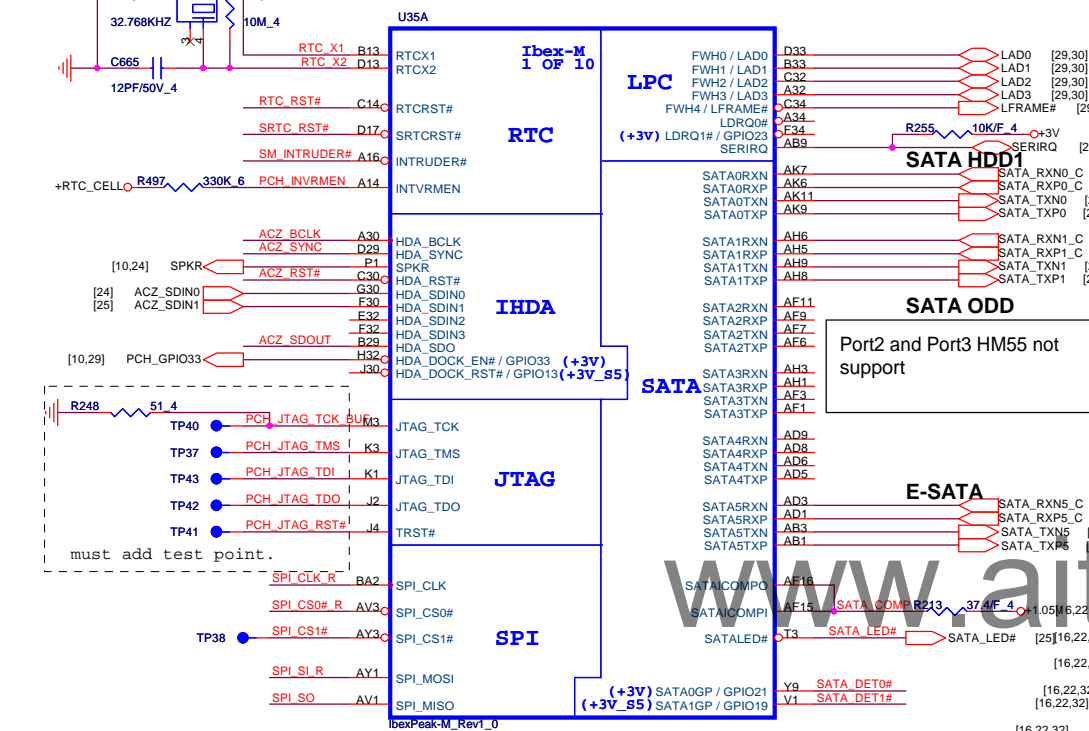
CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

NB5	PROJECT : TW9D Quanta Computer Inc.	
	Size Custom	Document Number PROCESSOR 4/4(GND)
Date: Thursday, April 15, 2010		Sheet 6 of 43

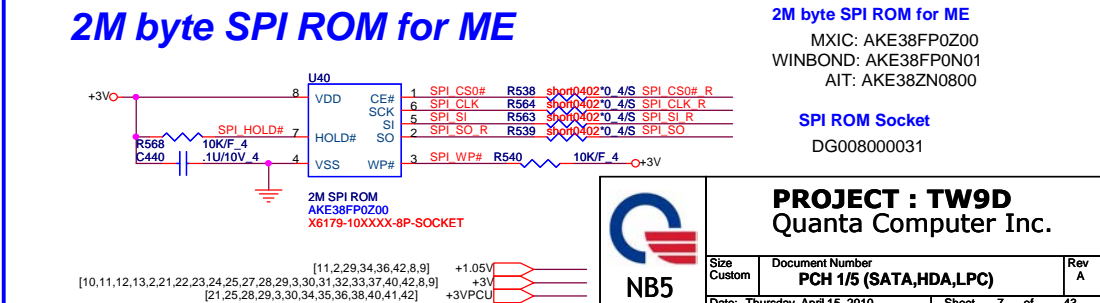
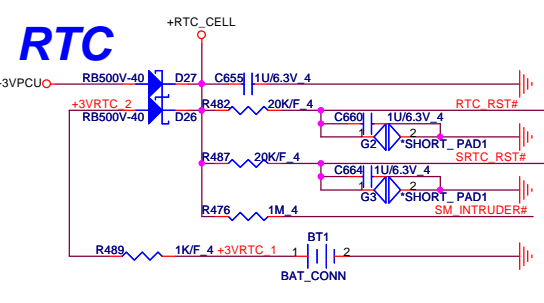
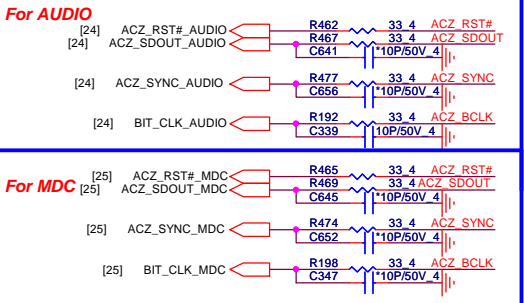
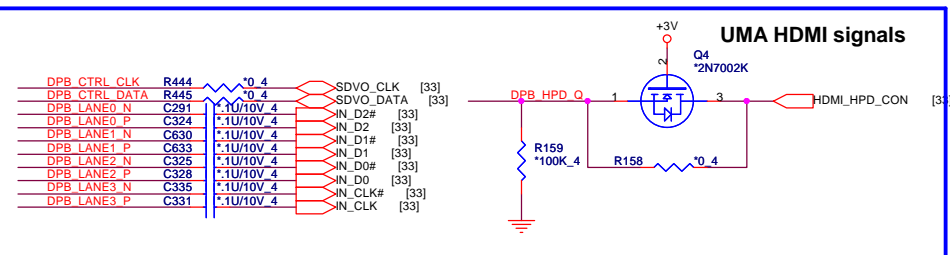
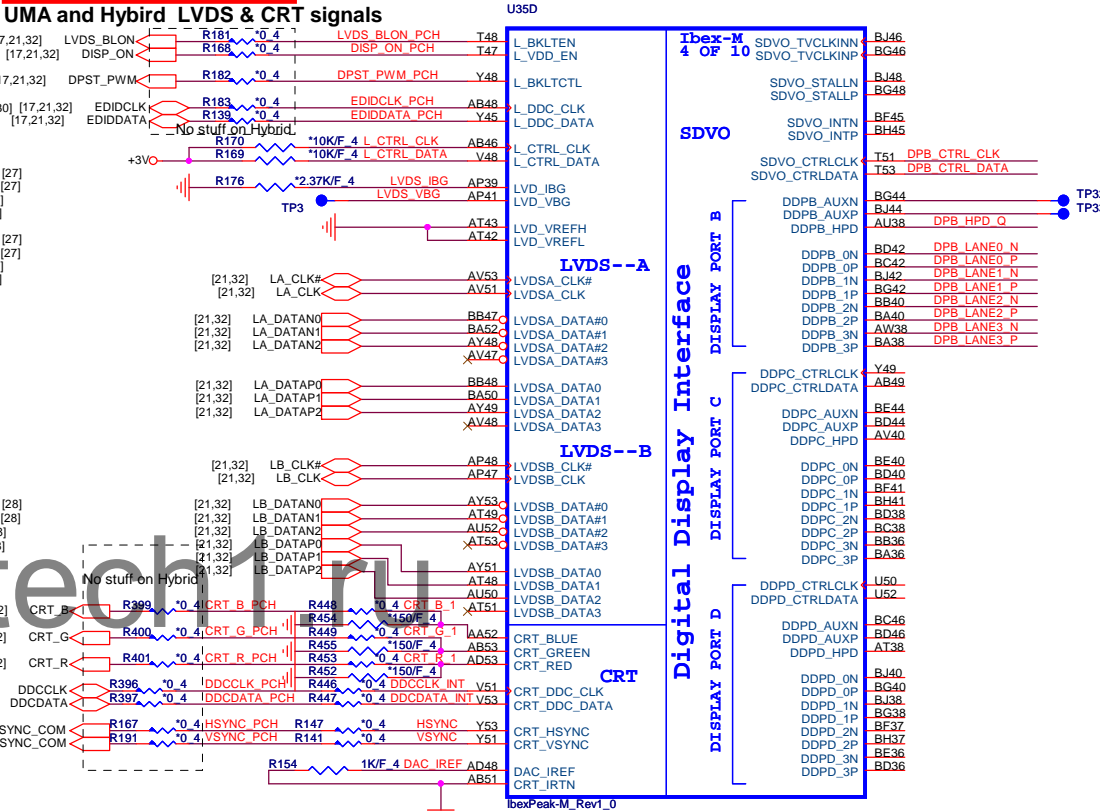
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)



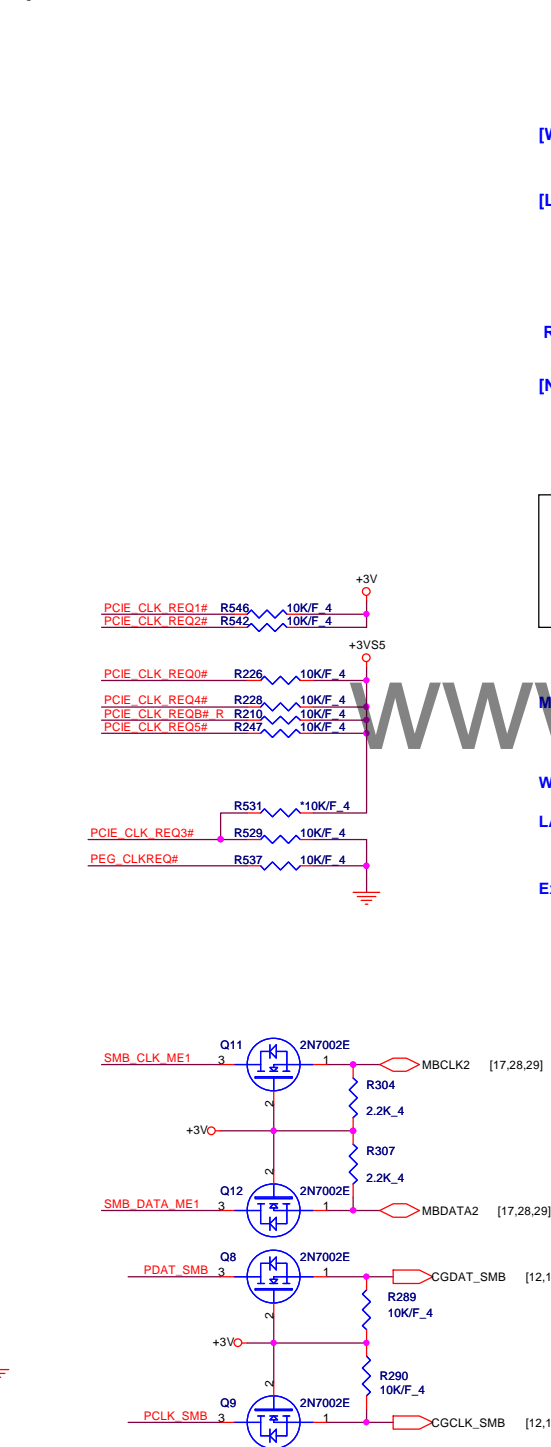
IBEX PEAK-M (LVDS,DDI)



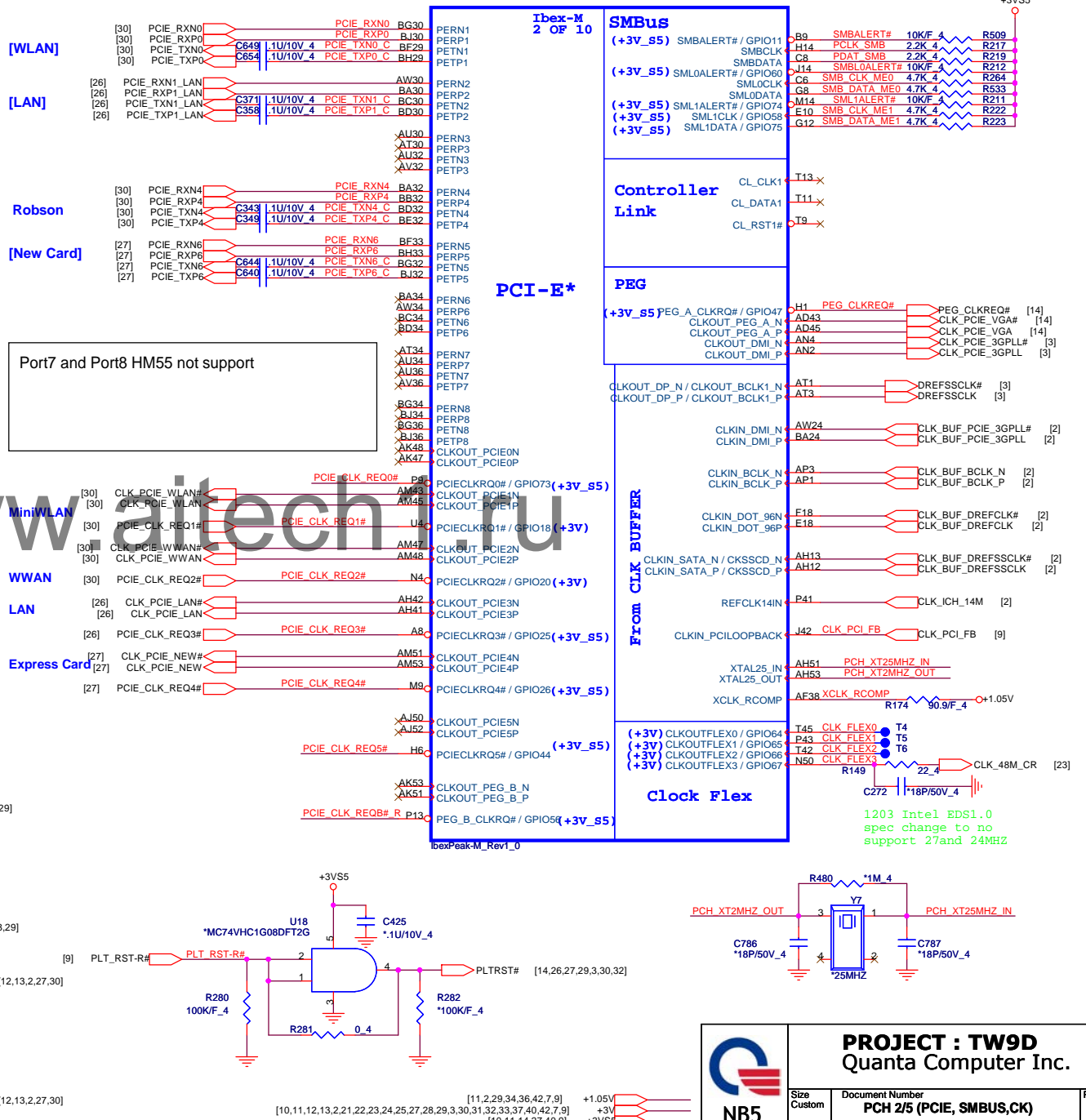
PROJECT : TW9D
Quanta Computer Inc.

Size Custom Document Number PCH 1/5 (SATA,HDA,LPC) Rev A

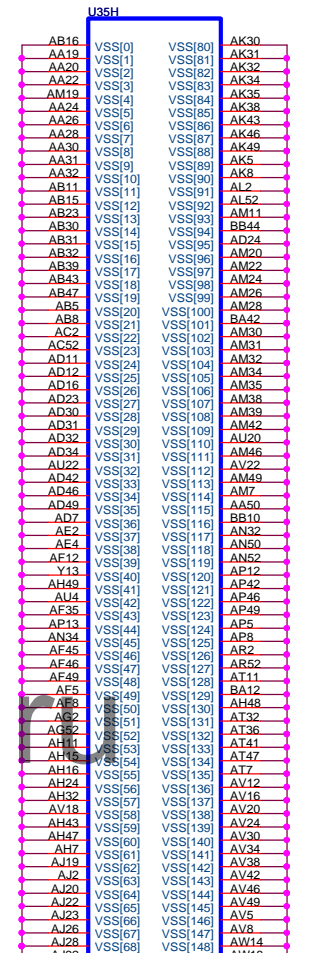
Date: Thursday, April 15, 2010 Sheet 7 of 43



U35B



10



BOARD ID SETTING


SETTING

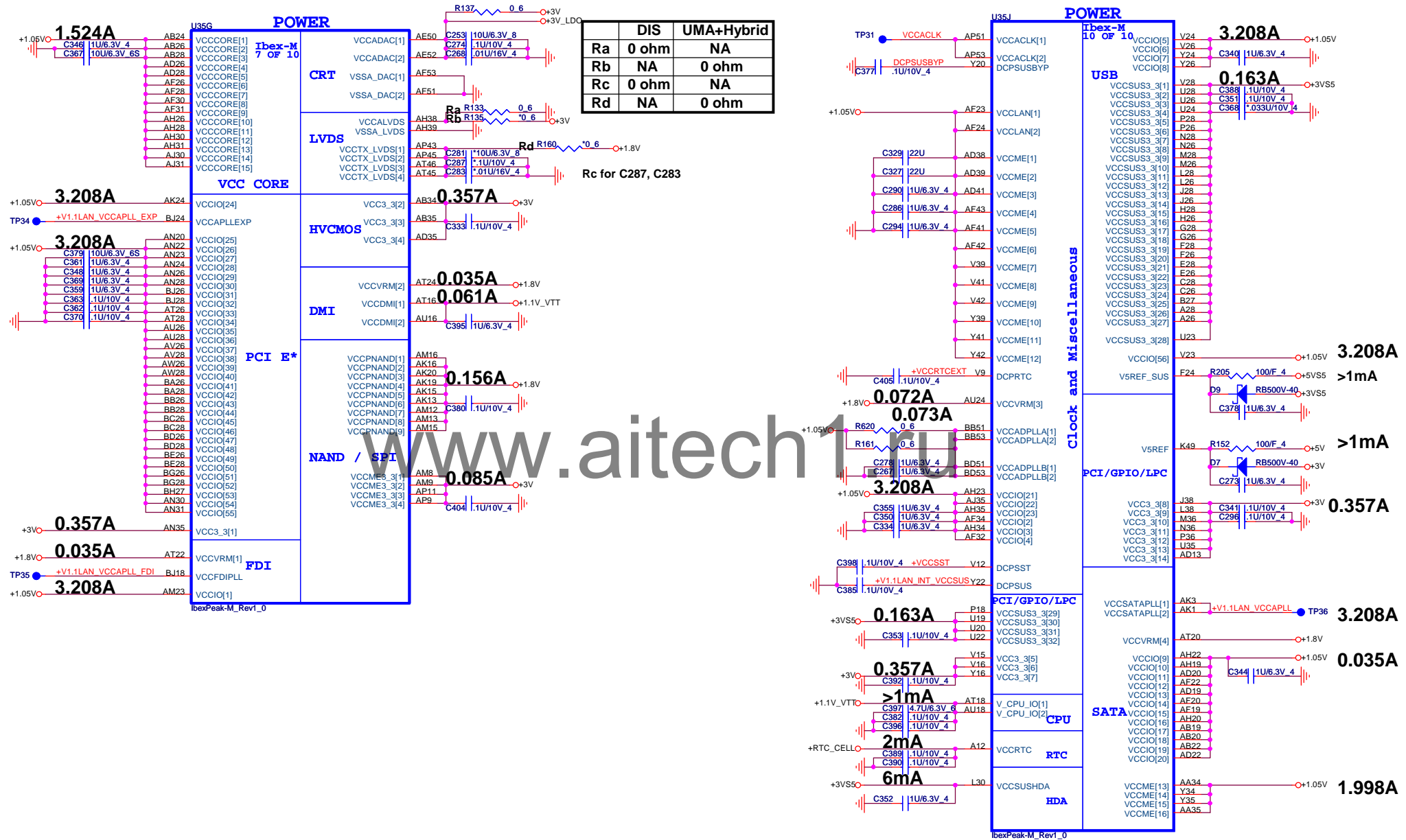
Pin connections for BOARD_ID6:

- [11,3,34,38,5] to +1.1V_VTT
- [11,31,36,40,42,5] to +1.8V
- [11,12,13,2,21,22,23,24,25,27,28,29,3,30,31,32,33,37,40,42,7,8,9] to +3V
- [11,14,27,40,8,9] to +3VSS

No Reboot Strap

[24,7] SPKR

 NB5	PROJECT : TW9D Quanta Computer Inc.		
	Size Custom	Document Number PCH 4/5 (GPIO & Strap)	Rev A
	Date: Thursday, April 15, 2010	Sheet 10 of 43	

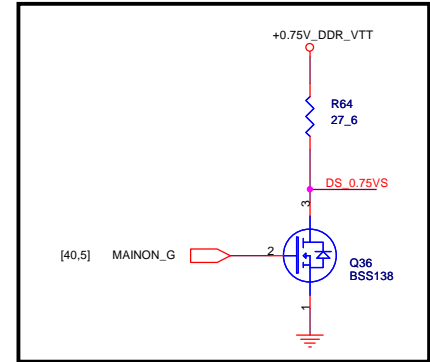
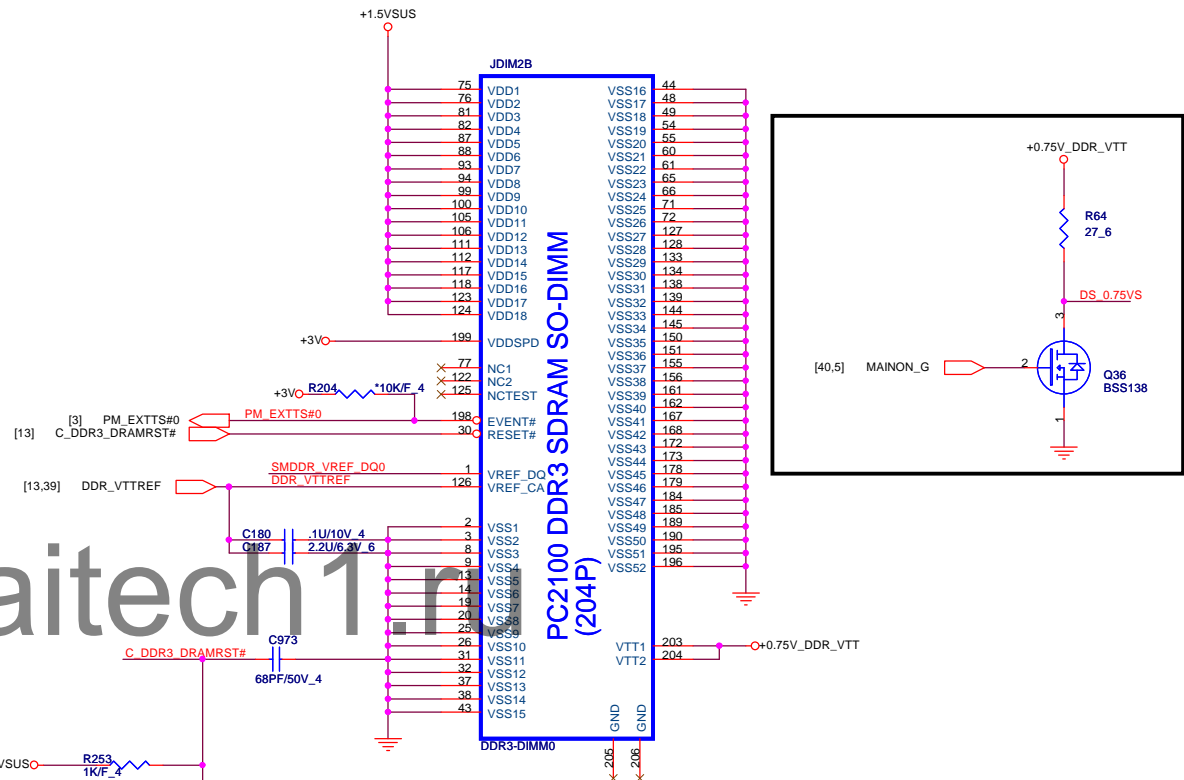
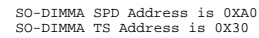


[2,29,34,36,42,7,8,9]	+1.05V
[10,3,34,38,5]	+1.1V_VTT
[10,31,36,40,42,5]	+1.8V
[10,12,13,2,21,22,23,24,25,27,28,29,3,30,31,32,33,37,40,42,7,8,9]	+3V
[10,14,27,40,8,9]	+3VSS
[22,24,25,27,28,30,32,40]	+5V
[40]	+5VSS

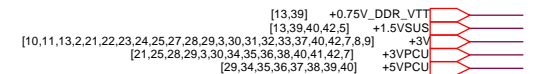
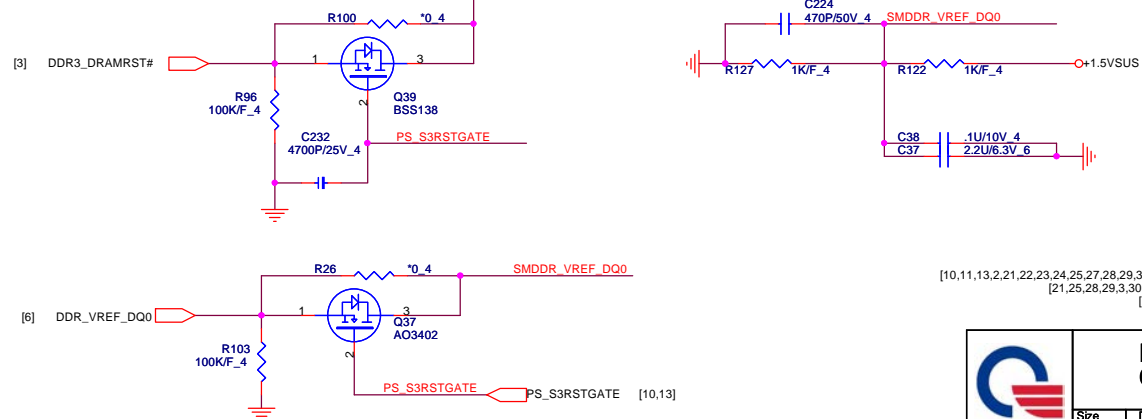
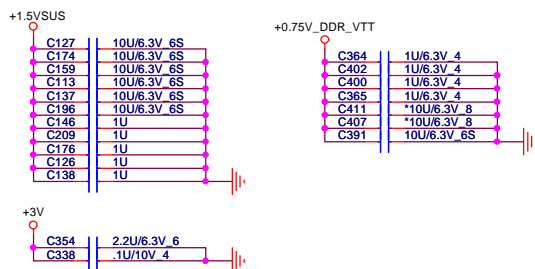


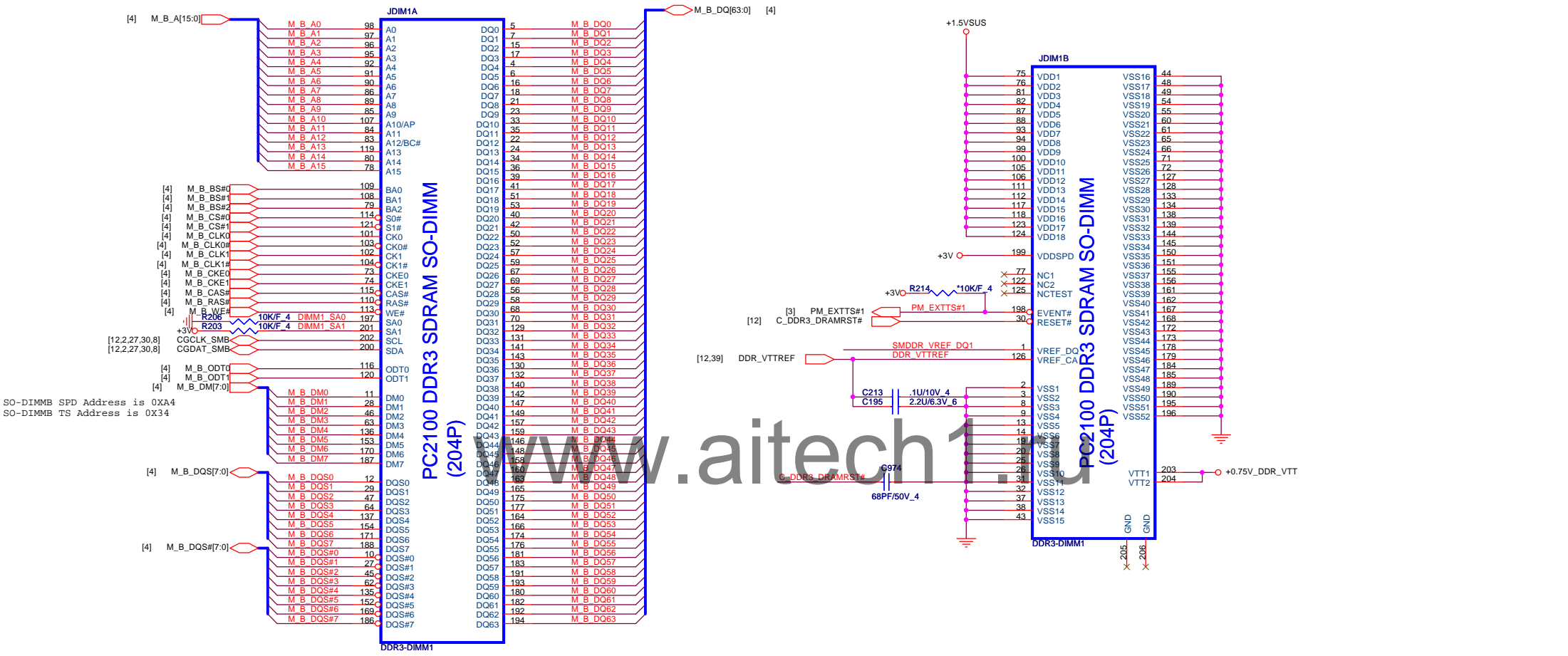
PROJECT : TW9D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	A
Date: Thursday, April 15, 2010		Sheet 11 of 43



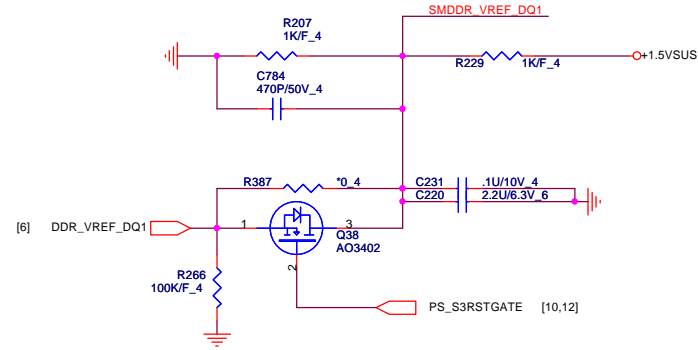
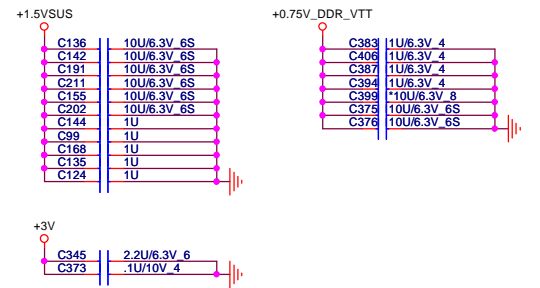
Place these Caps near So-Dimm0.





SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

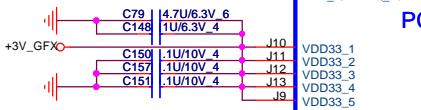
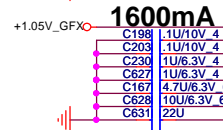
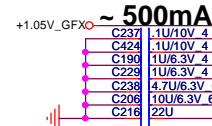
Place these Caps near So-Dimm1.



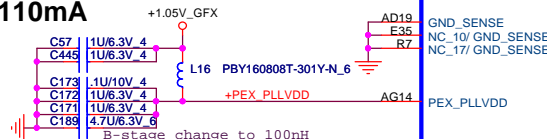
[12,39] +0.75V_DDR_VTT
[12,39,40,42,5] +1.5VSUS
[10,11,12,21,22,23,24,25,27,28,29,3,30,31,32,33,37,40,42,7,8,9] +3V
[21,25,28,29,3,30,34,35,36,38,40,41,42,7] +3VPCU
[29,34,35,36,37,38,39,40] +5VPCU

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD > 2.2A

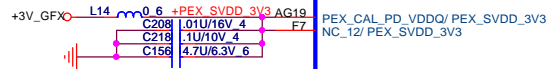
U33A
BGA489-NV/DIA-NB9P-GS
COMMON



**12~16 mils width
110mA**

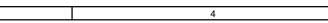
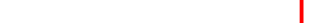
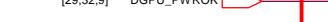
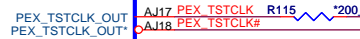
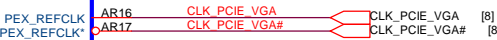
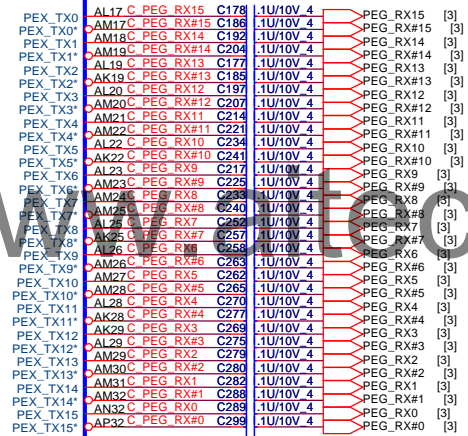
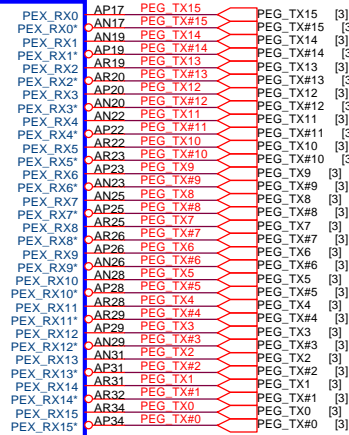


12~16 mils width



AG20 PEX_CAL_PU_GND/ NC
A2 NC.1
AB7 NC.2
AD6 NC.3
AF6 NC.4
AJ5 NC.5
AK15 NC.6
AL7 NC.7
E7 NC.8
H32 NC.13
M7 NC.14
P6 NC.15
U7 NC.18
V6 NC.19

PCI EXPRESS



Only for Hybrid

Only for Hybrid

Only for Hybrid

Only for Hybrid

Only for Hybrid

Only for Hybrid

Only for Hybrid

Only for Hybrid

Only for Hybrid

Only for Hybrid

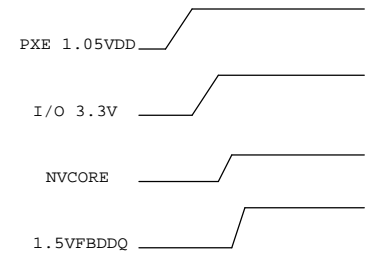
Only for Hybrid

Only for Hybrid

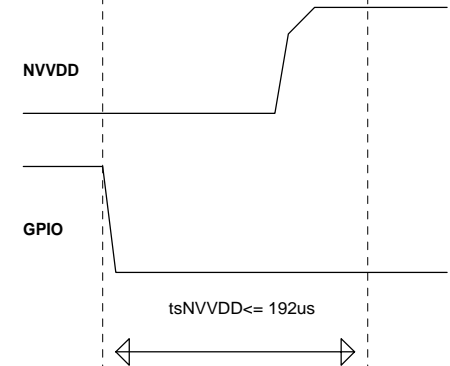
Only for Hybrid

Only for Hybrid

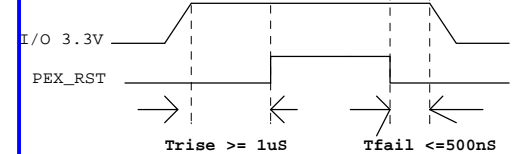
power up sequence



**NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time**



PEX_RST timing

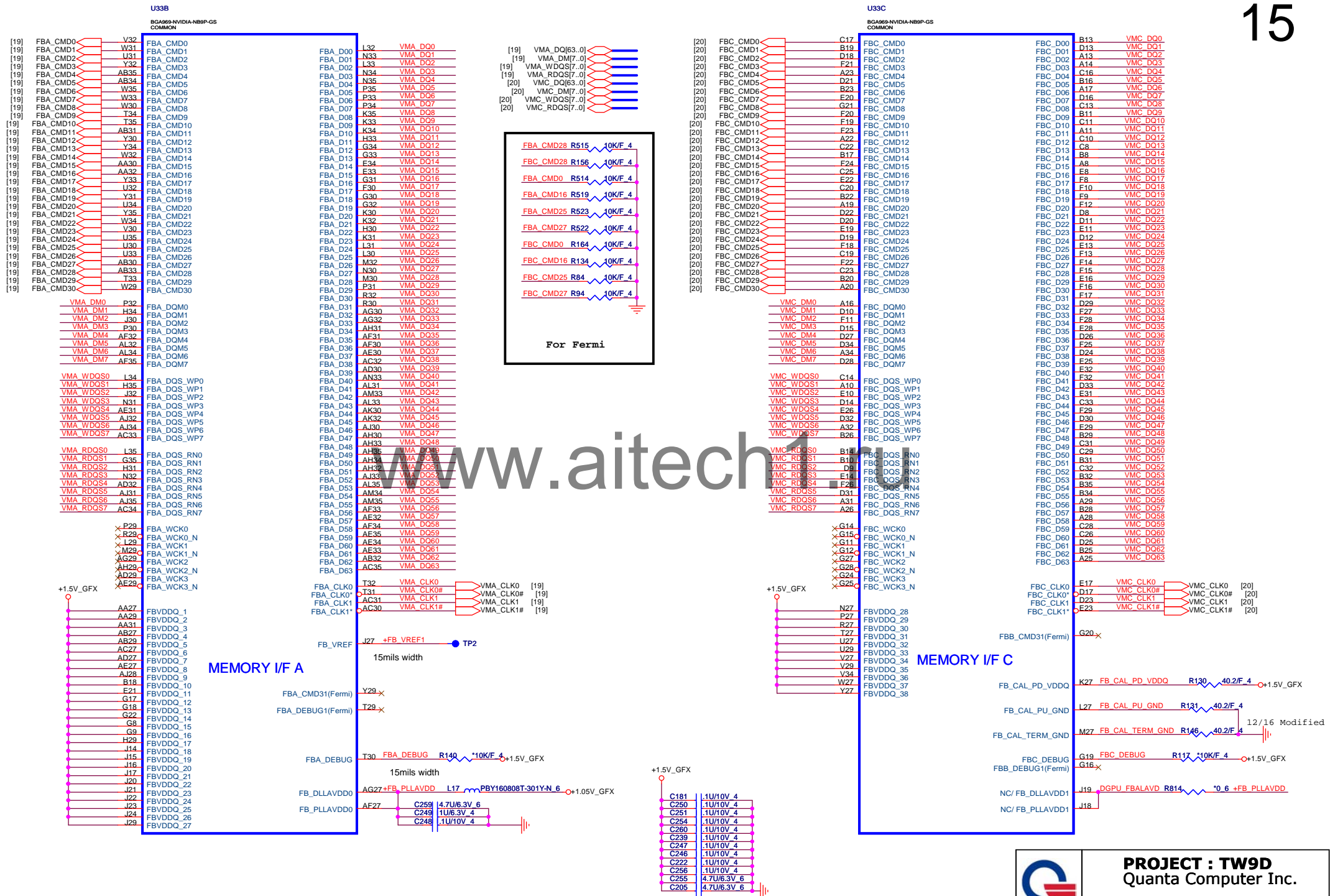


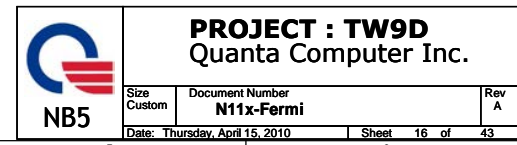
[15,16,32,42] +1.05V_GFX
[16,17,22,32,33,38,42] +3V_GFX

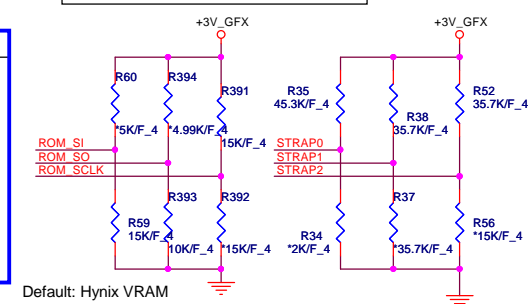


PROJECT : TW9D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N11x-Ferri	A
Date: Thursday, April 15, 2010	Sheet 14 of 43	







4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
 10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
 15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
 30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
 35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]
 20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
01	0000		Reserved		
02	0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
	0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
	0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
	0101		Reserved		
	0110				
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

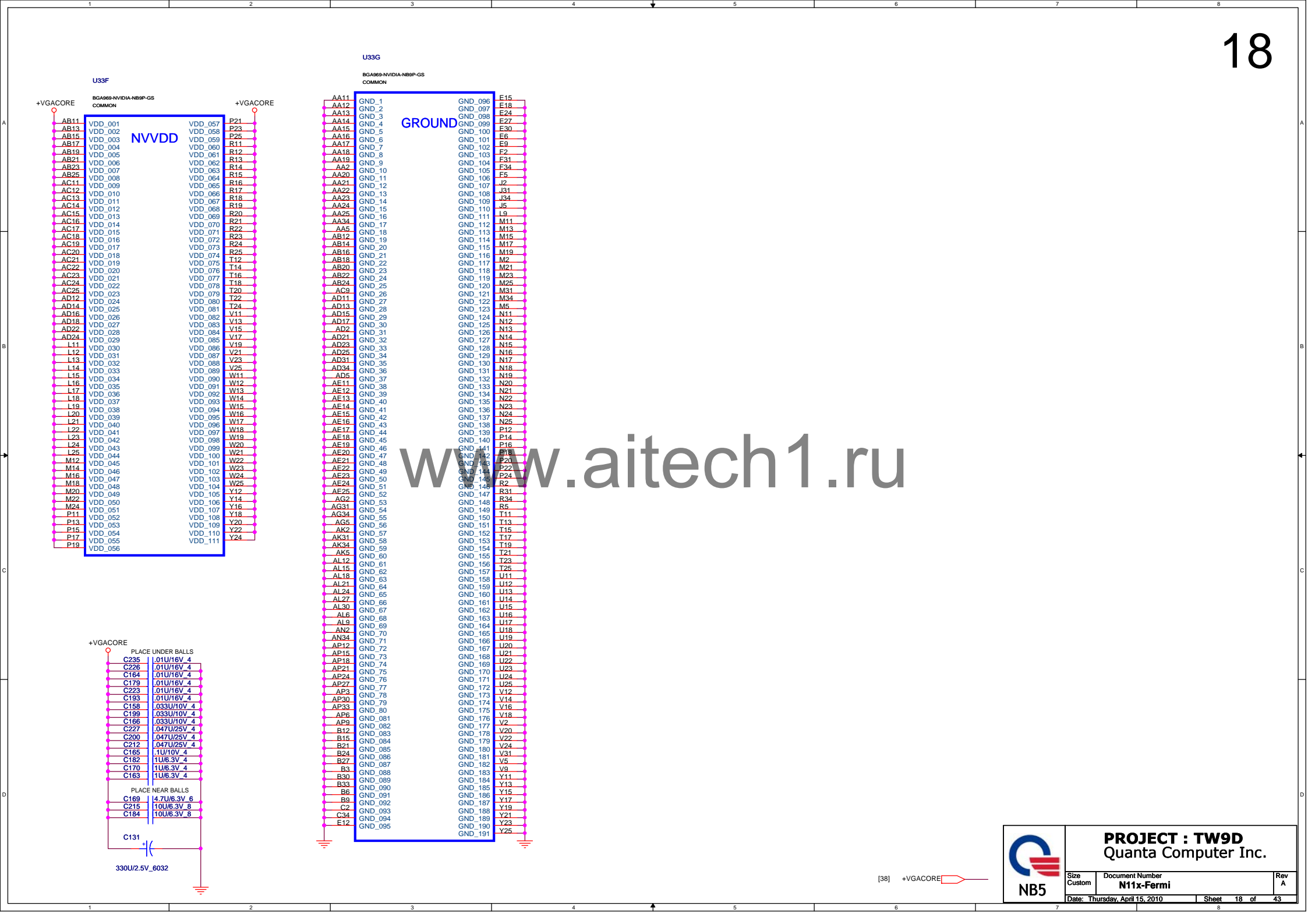
GPIO ASSIGNMENTS

GPI/O	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

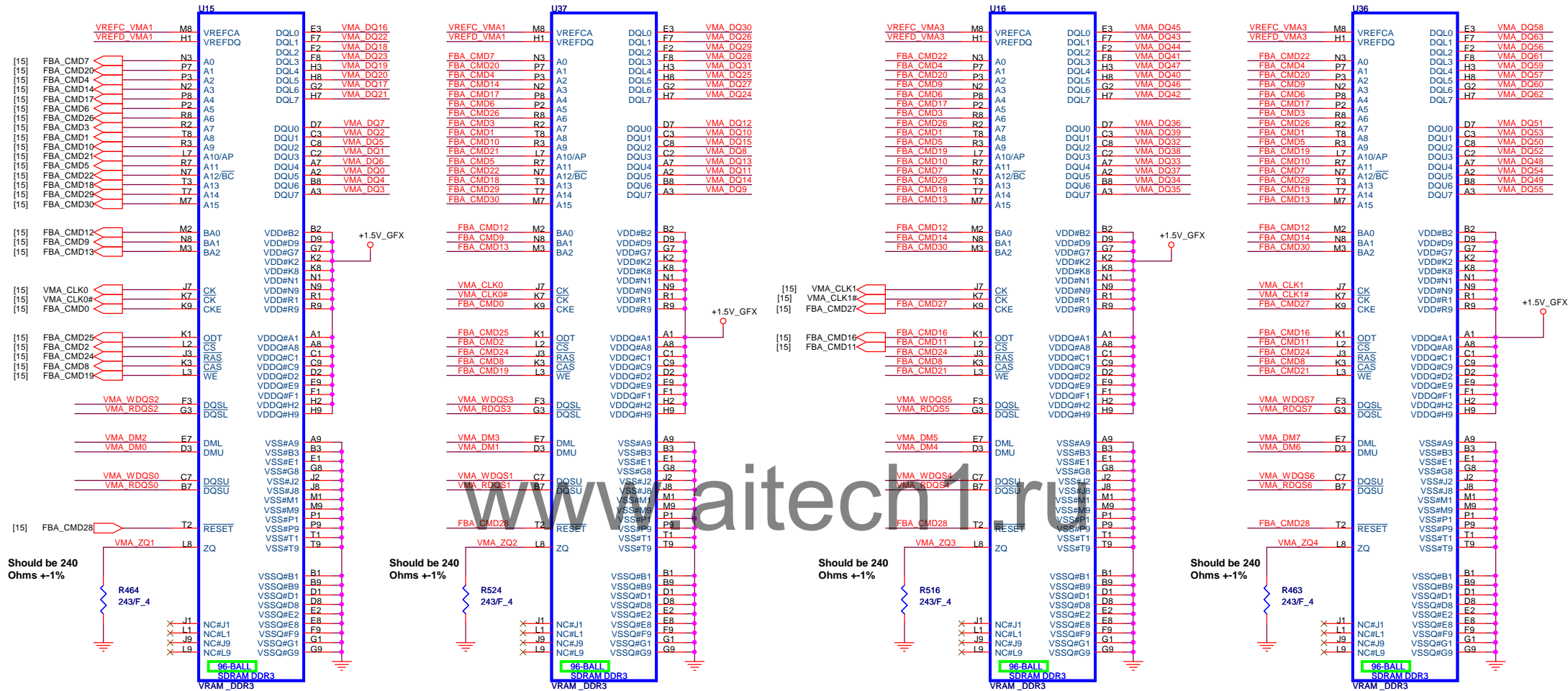


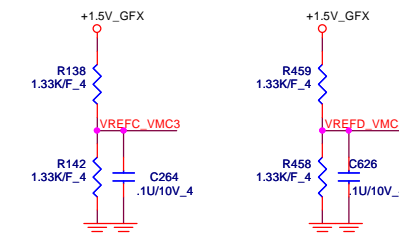
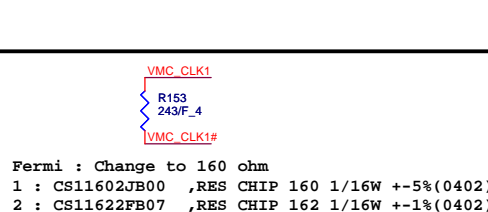
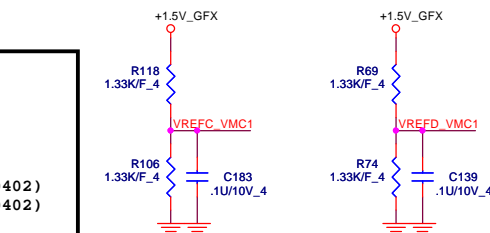
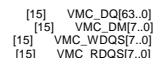
PROJECT : TW9D
Quanta Computer Inc.

Size Custom	Document Number N11x-Fermi	Rev A
Date: Thursday, April 15, 2010		Sheet 17 of 43



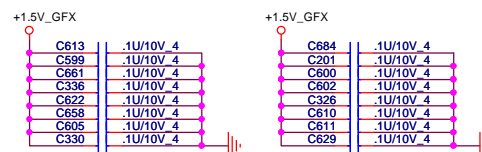
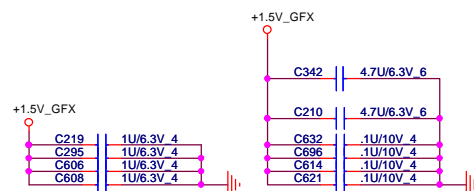
CHANNEL A: 256MB/512MB DDR3





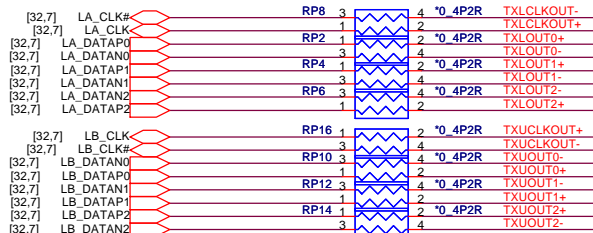
```
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)
```

```
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402
```

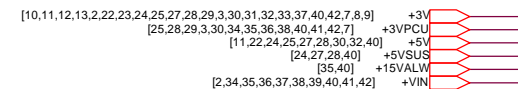
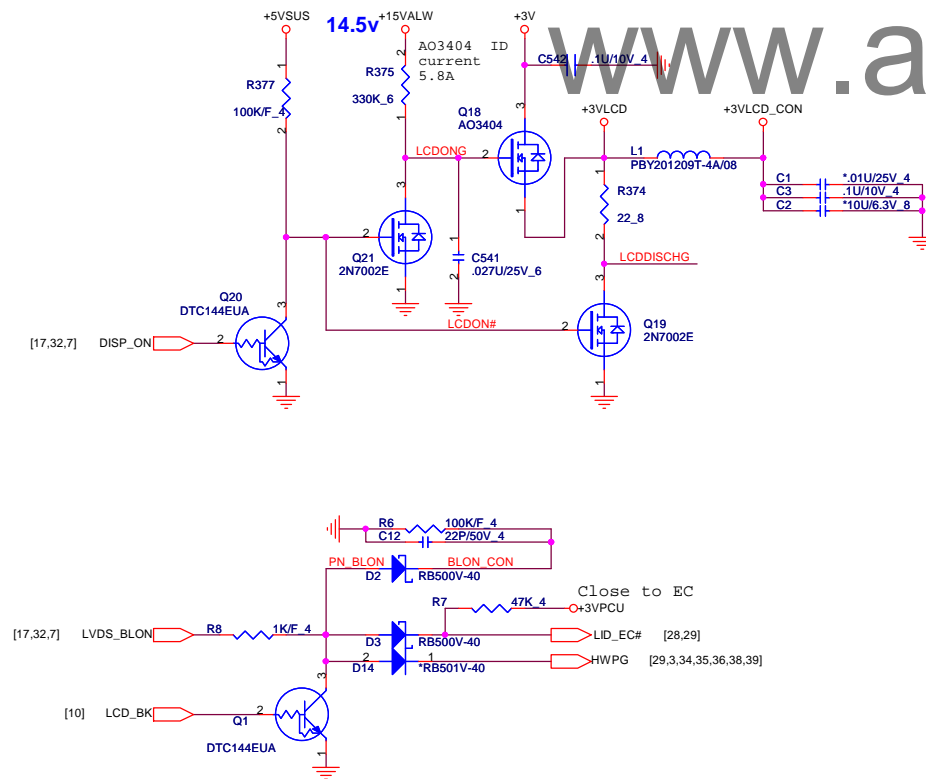
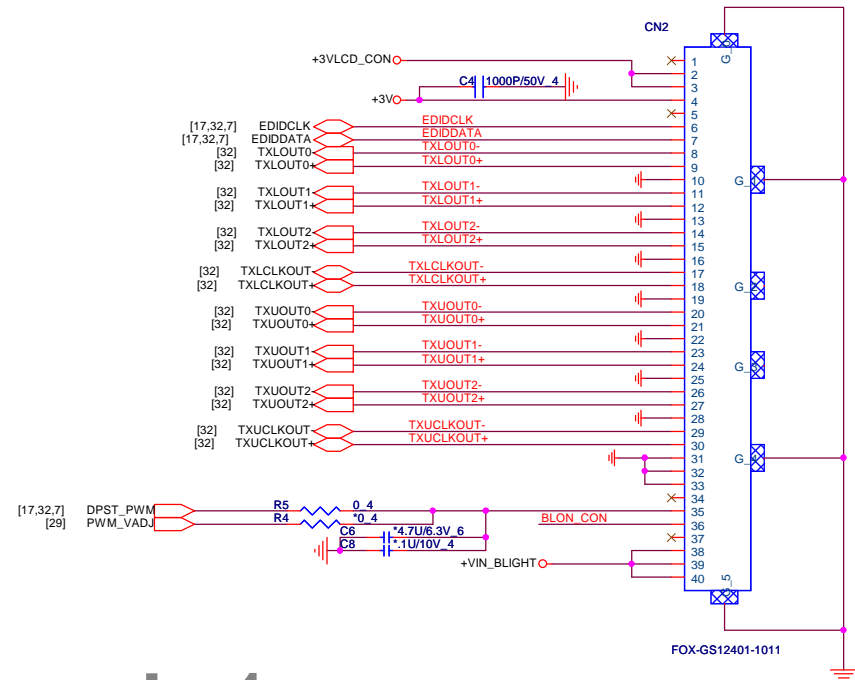
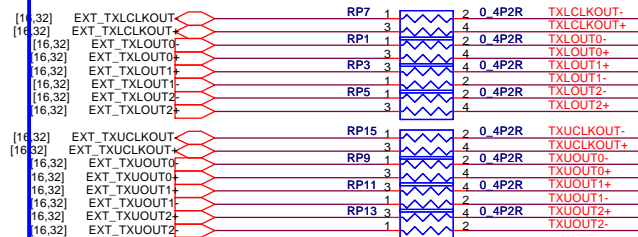


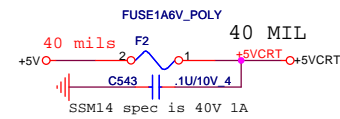
1. If LCD connector near GPU, then place these series Resistors near GPU
 2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

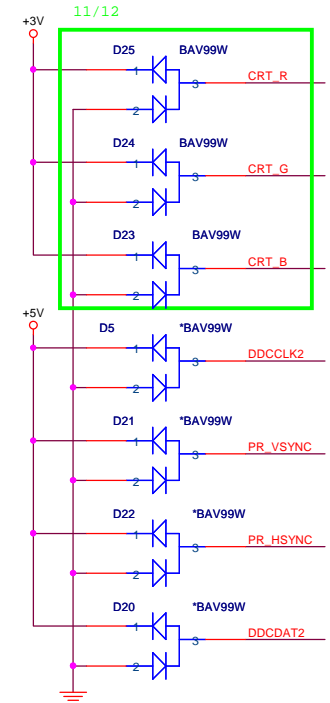
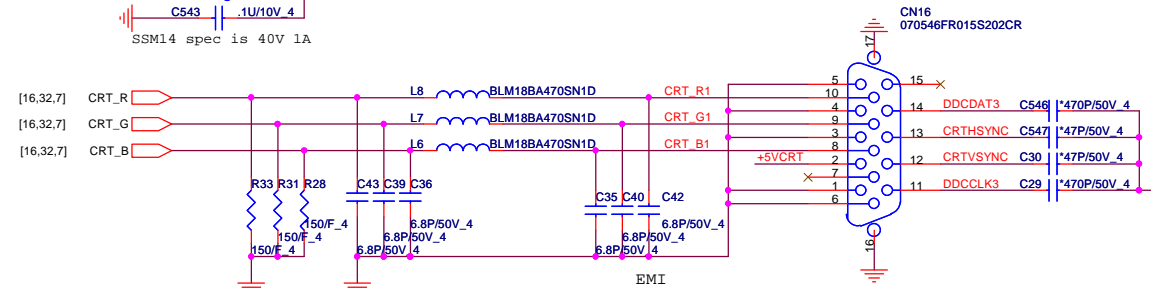


OPTION SIGNAL FROM Nvidia to VGA





CRT PORT



For EMI

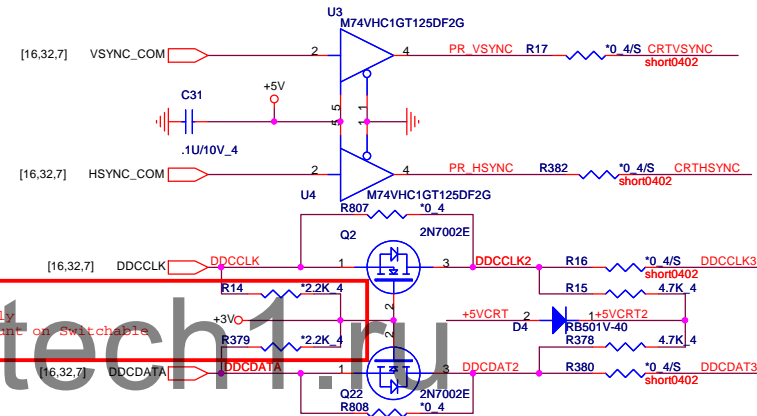
C TX2_HDMI+ R616 *0.4 C TX2_HDMI-

C TX1_HDMI+ R616 *0.4 C TX1_HDMI-

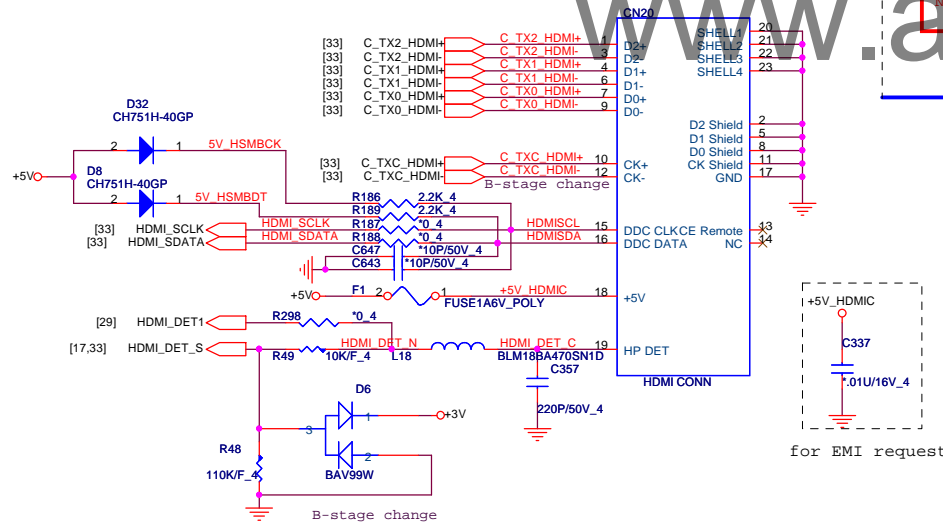
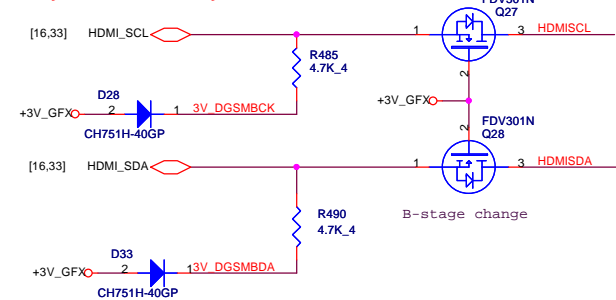
C TX0_HDMI+ R617 *0.4 C TX0_HDMI-

C TXC_HDMI+ R619 *0.4 C TXC_HDMI-

HDMI PORT



Only for Discrete and Hybrid



R187 / R188 for Switchable / UMA



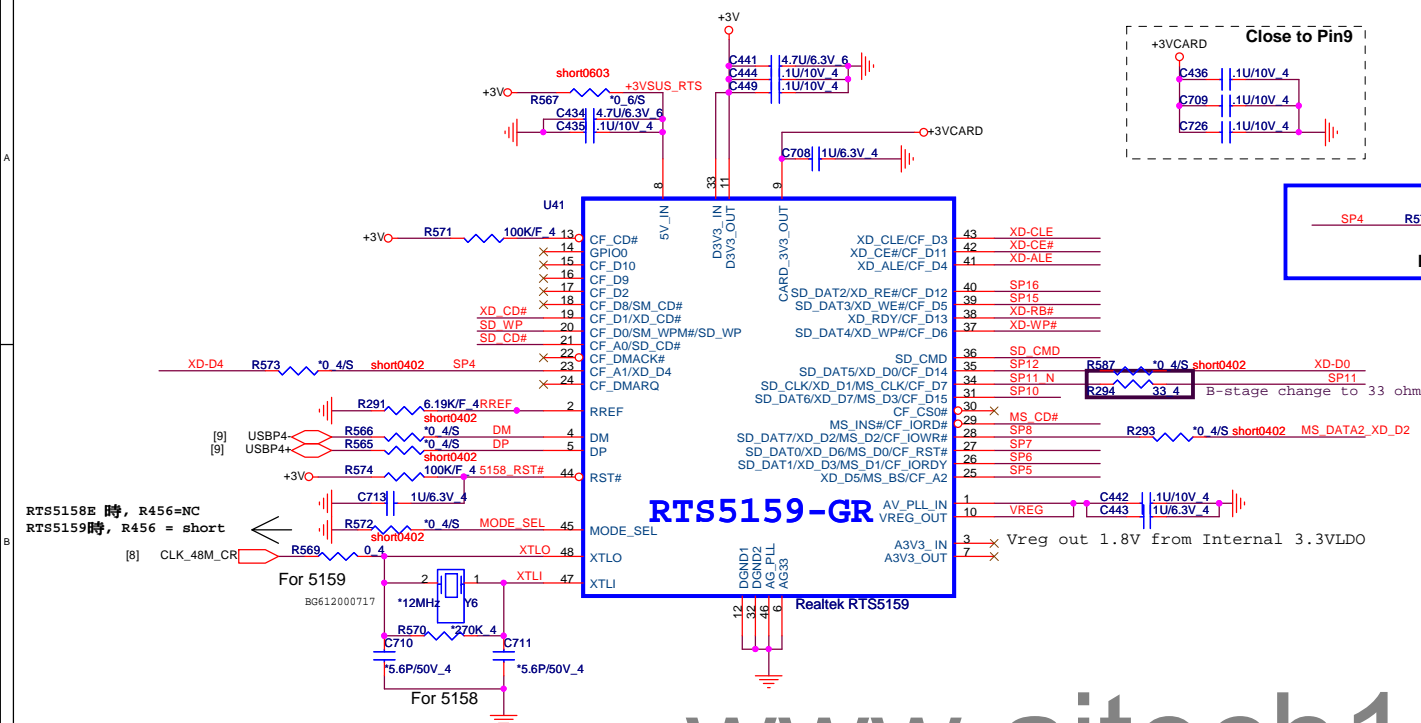
PROJECT : TW9D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	A
Date: Thursday, April 15, 2010	Sheet 22 of 43	

[10,11,12,13,21,23,24,25,27,28,29,30,31,32,33,37,40,42,7,8,9]
[11,24,25,27,28,30,32,40]

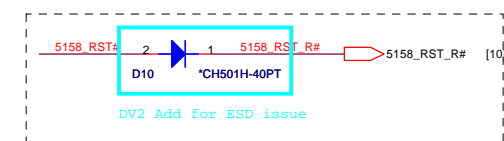
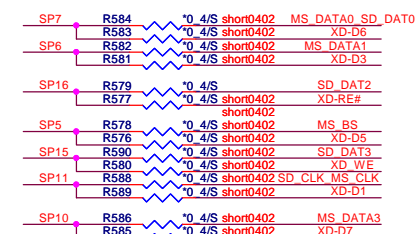
+3V
+5V

Note:



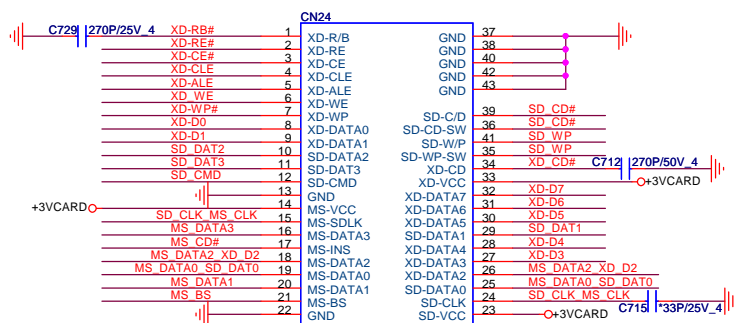
	SD/MMC	MS	XD
SP0			
SP1			XD CD#
SP2	SD WP		
SP3	SD CD#		
SP4	SD DAT1		
SP5		MS BS	XD D4
SP6		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD R/B#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE

For RTS5159



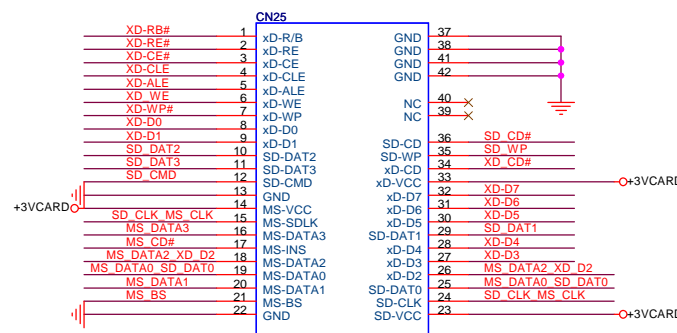
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5 IN1 CARD READER
XD,MMC/SD,MS/MSP

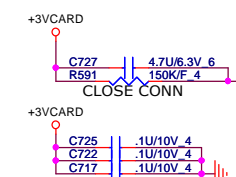


5IN1 CARD READER SOCKET

PV change footprint



*TAI TWUM 5IN1 CARD READER SOCKET
PV change footprint



PROJECT : TW9D
Quanta Computer Inc.

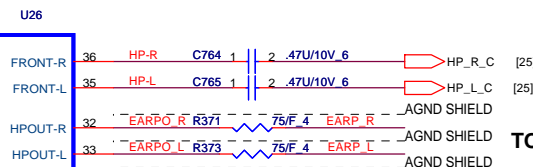
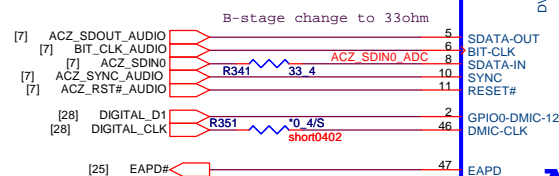
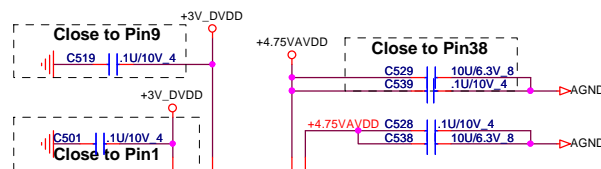
Size	Document Number
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Custom	RTS5159 & CR SOCKET
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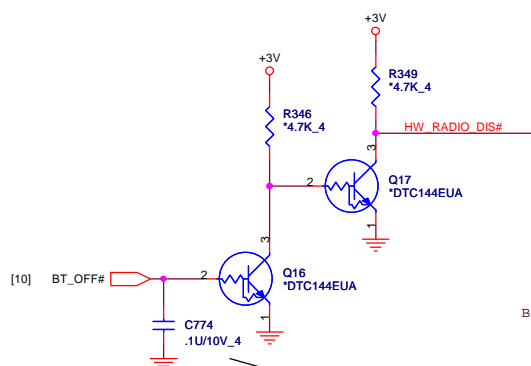
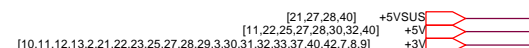
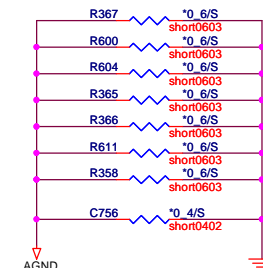
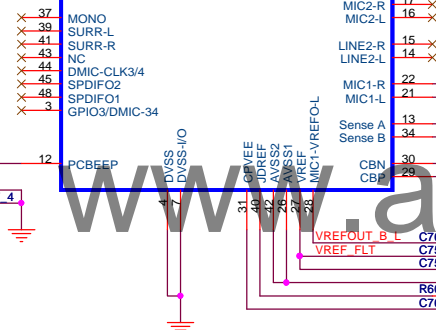
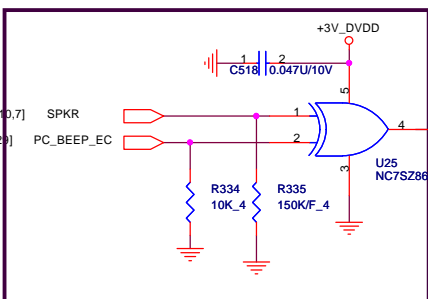
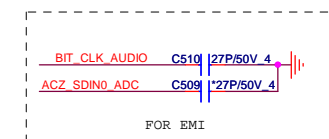
Rev

A

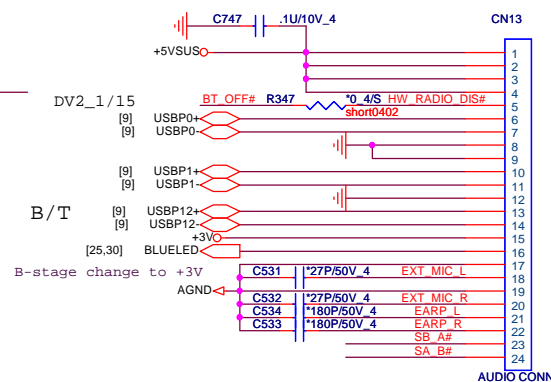
Date: Thursday, April 15, 2010	Sheet 23 of 43
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TO Internal Speakers

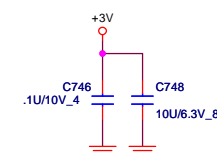
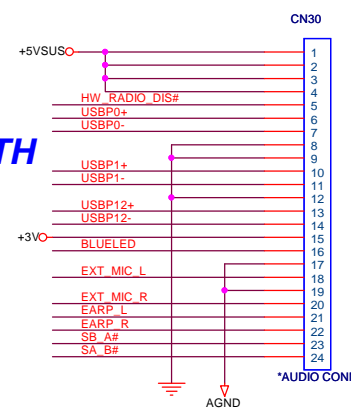


For EMI Request



BLUETOOTH

Audio



SB_A# -->EXT HP

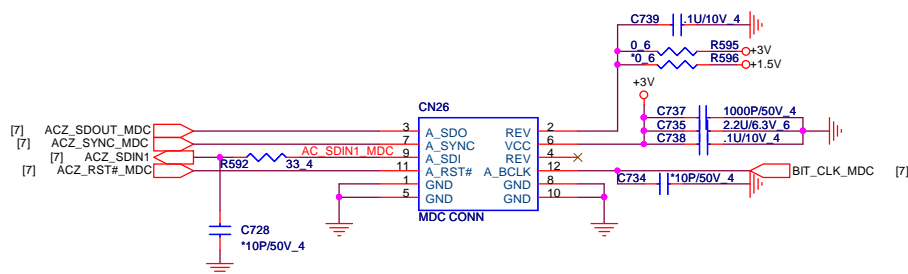
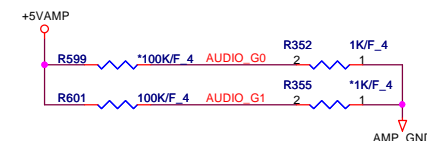
SA_B# -->EXT MIC

Audio JACK: Normal Open

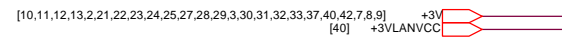
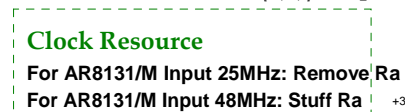


PROJECT : TW9D
Quanta Computer Inc.

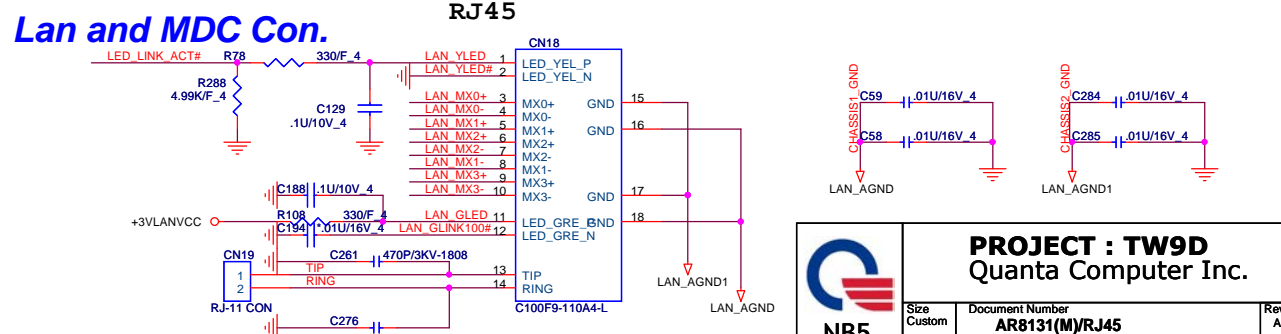
Size Custom	Document Number Azalia ALC272/BT CONN	Rev A
Date: Thursday, April 15, 2010		Sheet 24 of 43



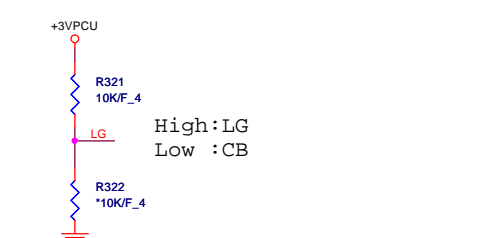
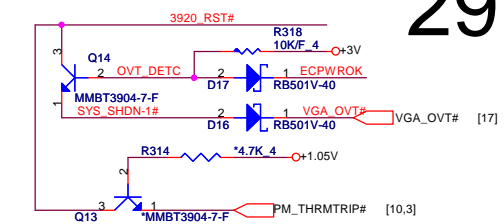
$$I = V_{CC} - V_f / R$$



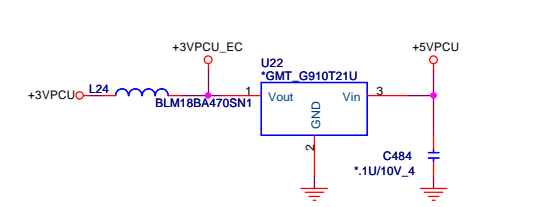
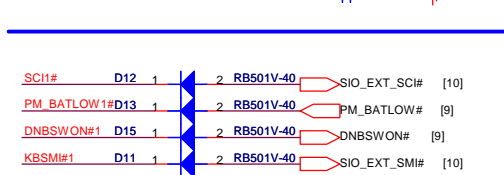
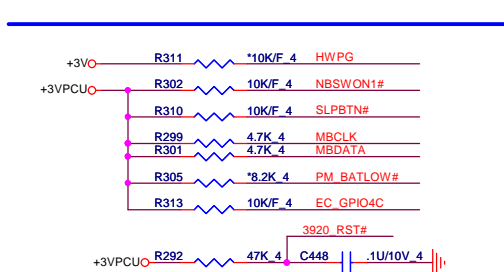
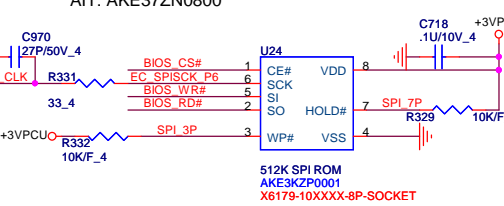
Lan and MDC Con.



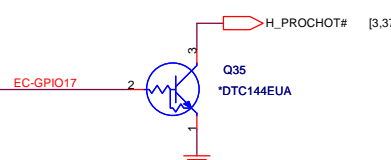
thermal shutdown circuit



SPI BIOS
512K byte SPI ROM for EC SPI ROM Socket
MXIC: AKE3KZP0001 DG008000031
WINBOND: AKE37ZN0N00
AIT: AKE37ZN0800

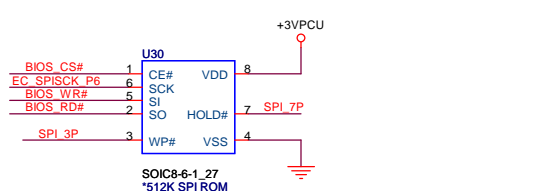


D30
RB501V-40
DGPU_HOLD_RST# 1 2 OVT_DET#
1 : For switchable
2 : Un-mount D17

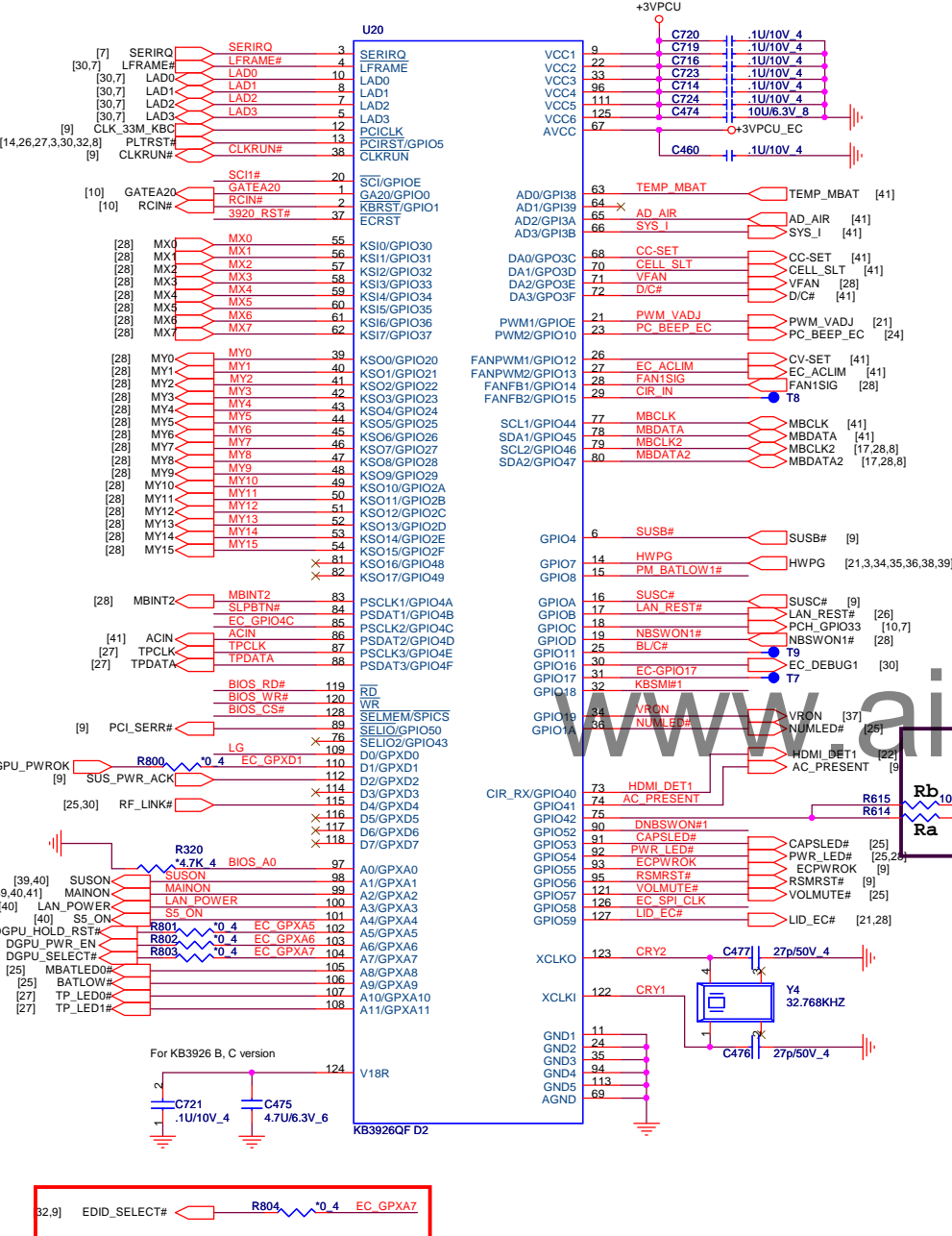
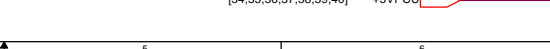


Adapter table select

ID	Ra	Rb
120W	10K	N/A
65W/90W	N/A	10K



[10,11,12,13,21,22,23,24,25,27,28,30,31,32,33,37,40,42,7,8,9]
[21,25,28,30,34,35,36,38,40,41,42,7]
[34,35,36,37,38,39,40]

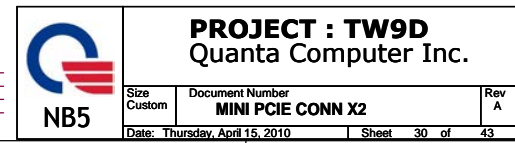


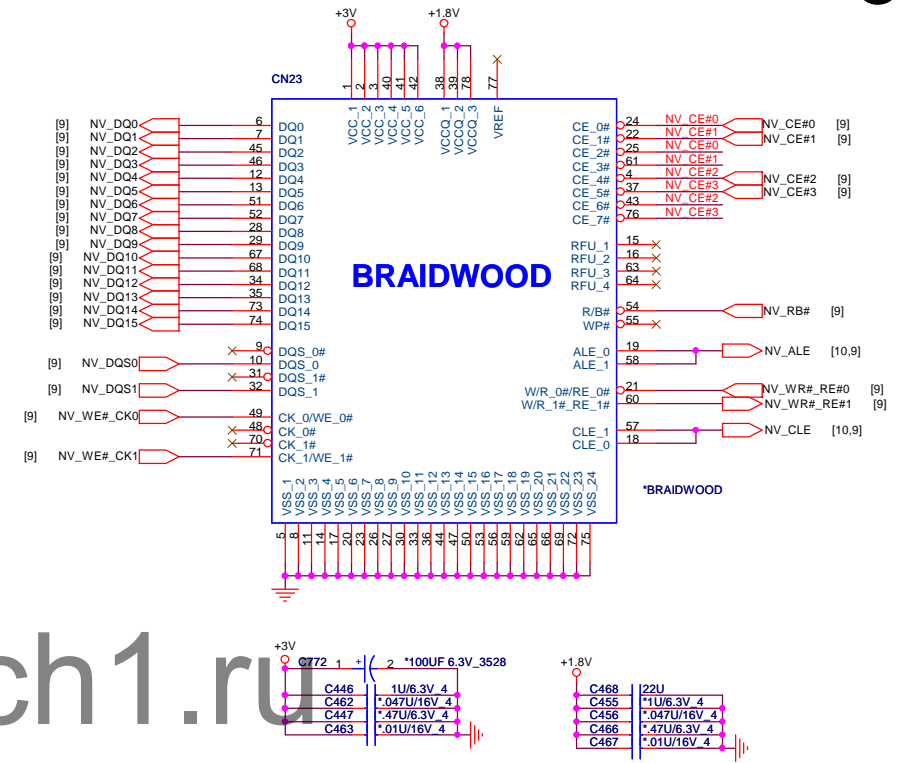
32,9] EDID_SELECT# R804 *0.4 EC_GPXA7

30

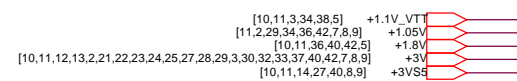


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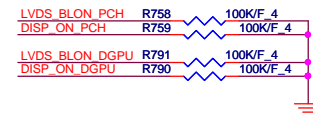
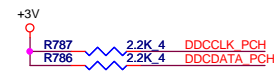
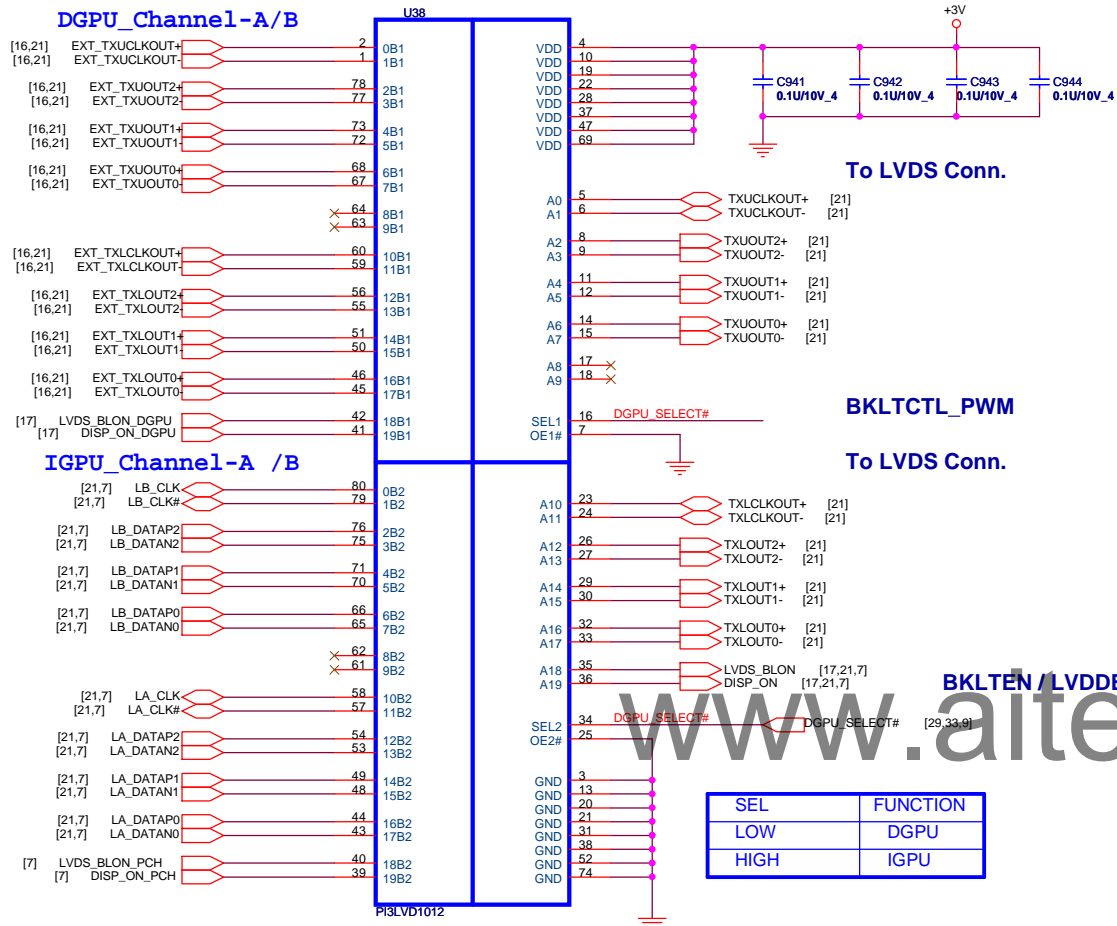




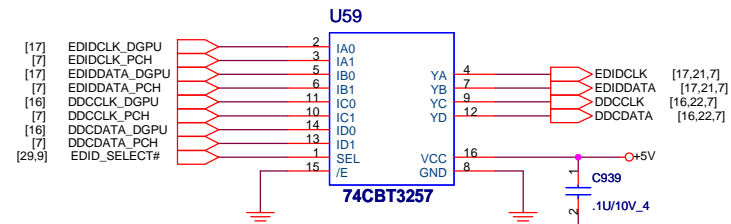
www.aitech1.ru



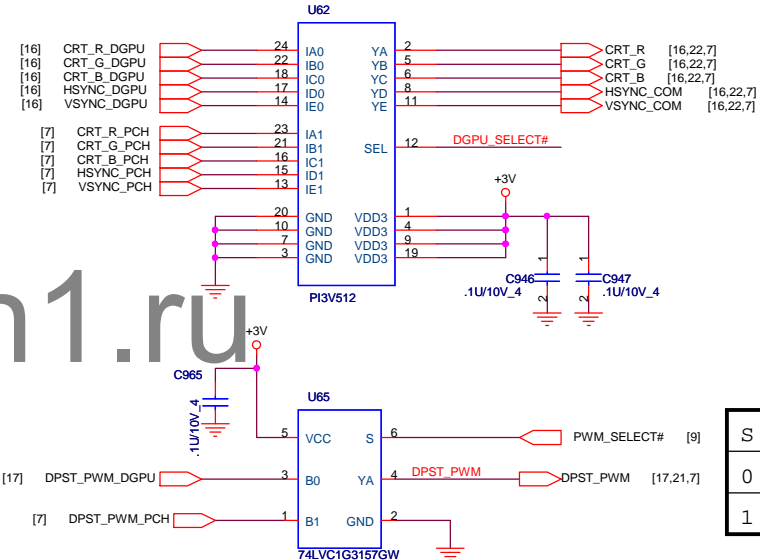
LVDS Channel Switch



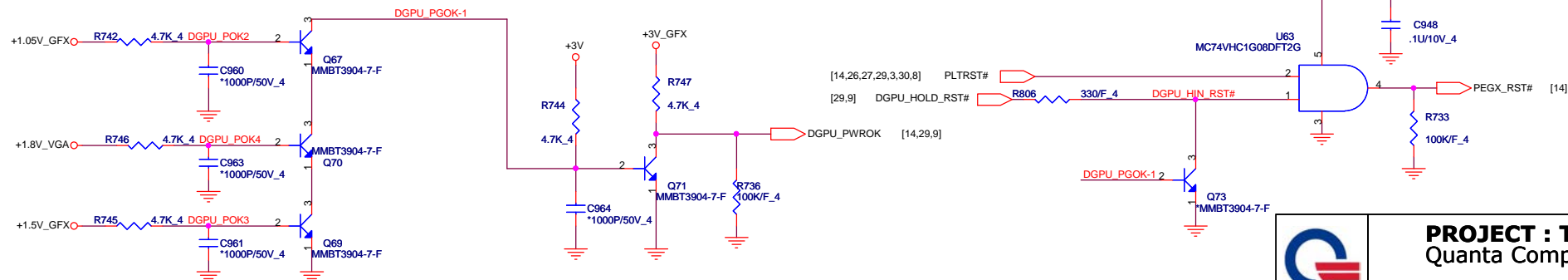
LVDS/CRT DDC Switch



VGA SWITCH

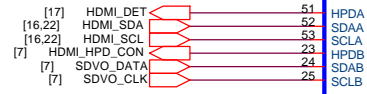
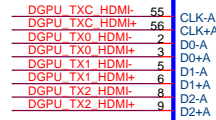
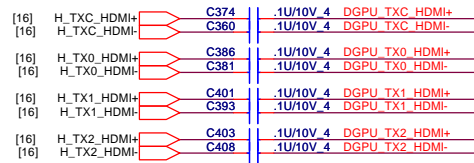


S	Yn
0	B0
1	B1

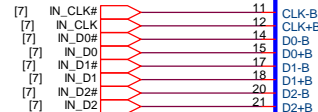


PROJECT : TW9D
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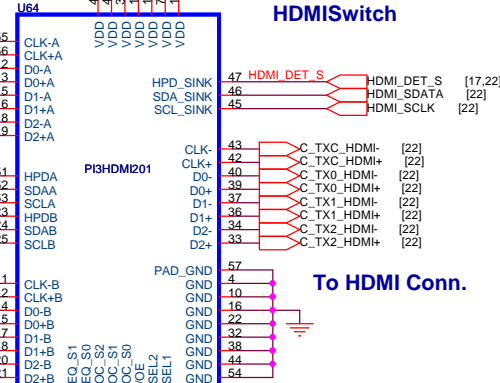
DGPU_HDMI



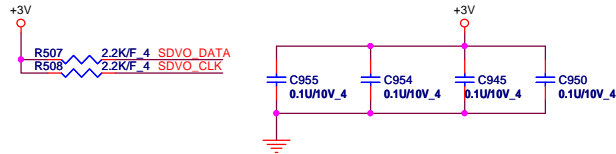
IGPU_HDMI



HDMI_SWITCH



To HDMI Conn.



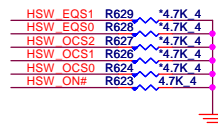
OC SETTING

S2 S1 S0 = 1 : 1 : 1 500mV 0dB Default
 S2 S1 S0 = 1 : 1 : 0 750mV 0dB
 S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
 S2 S1 S0 = 1 : 0 : 0 600mV 0dB
 S2 S1 S0 = 0 : 1 : 1 500mV 0dB
 S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
 S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
 S2 S1 S0 = 0 : 0 : 0 500mV 6dB

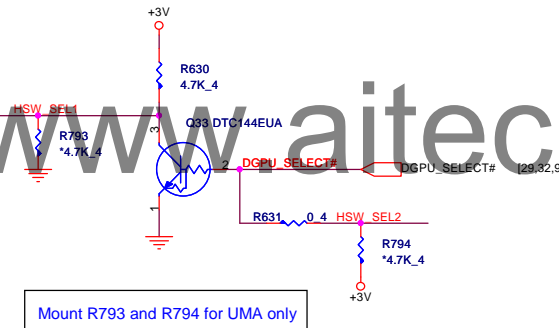
EQ SETTING

S1 S0 = 1 : 1 3dB Default
 S1 S0 = 1 : 0 8dB
 S1 S0 = 0 : 1 3dB
 S1 S0 = 0 : 0 15dB

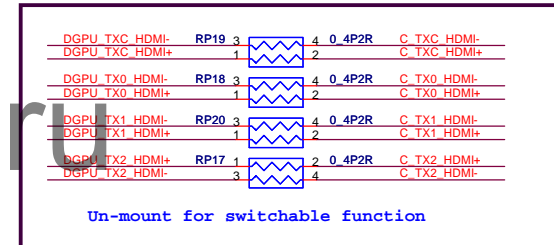
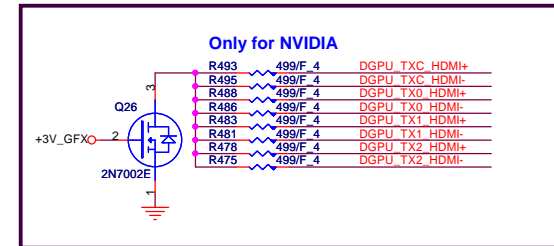
OE#	SEL2	SEL1	Ay
0	X	1	A
0	1	0	B



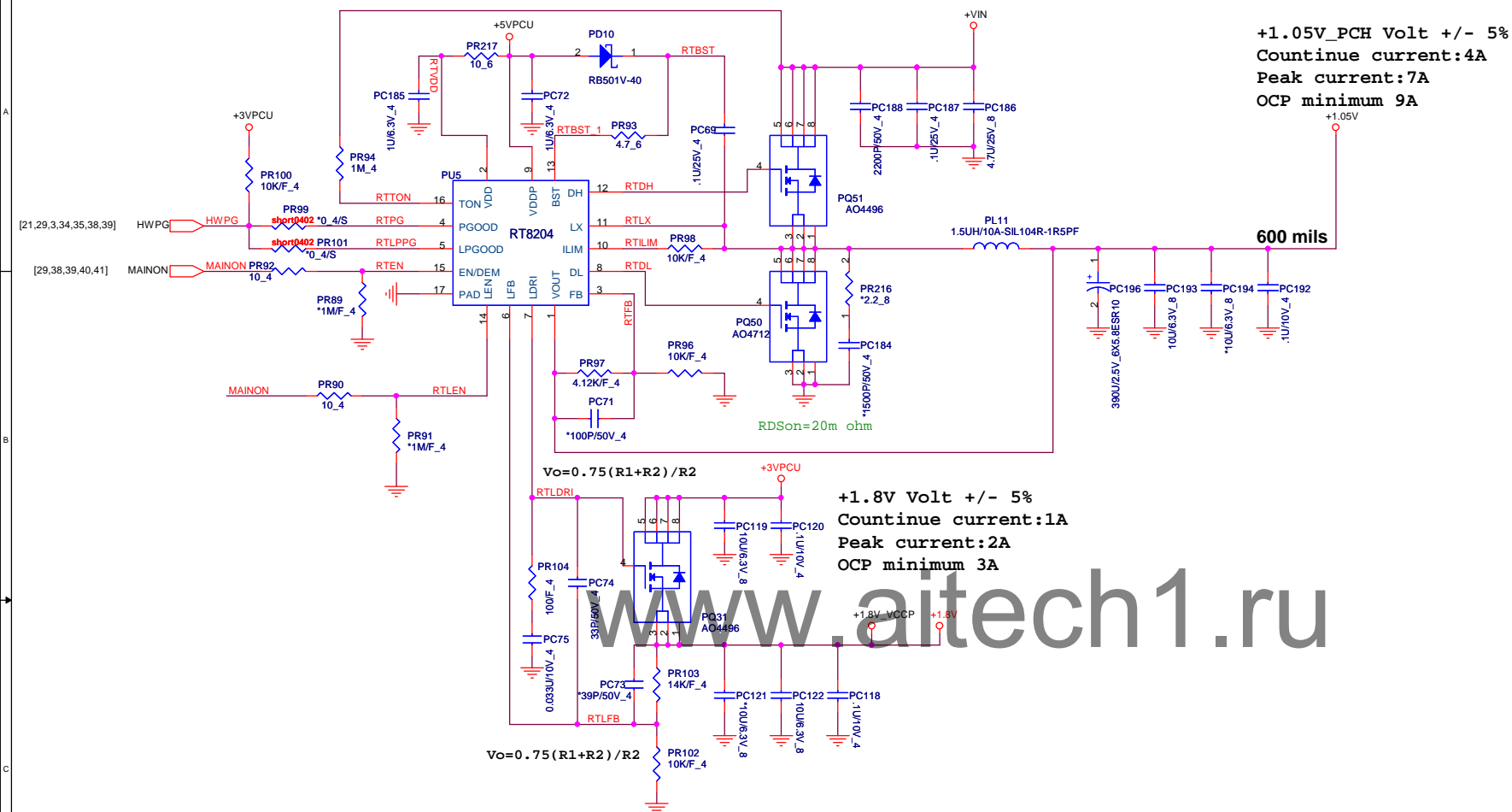
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Mount R793 and R794 for UMA only

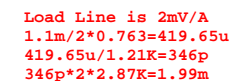


Un-mount for switchable function



PROJECT : TW9D
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Size Custom	Document Number PCH +1.05V (RT8204)	Rev A
Date: Thursday, April 15, 2010	Sheet 36 of 43	



OCP Setting	PR20	PR10
45W CPU (60A)	1.24K P/N: CS21242FB20	2.8K P/N: CS22802FB18
35W CPU (48A)	1.05K P/N:	2.37K P/N: CS22372FB11

OCP
 $40\mu\text{A}/2 \times 1.21\text{K} = 24.2\text{mV}$
 $24.4\text{mV}/0.763 = 31.72\text{mV}$
 $31.72\text{mV} \times 2/1.1\text{m} = 57.66\text{mV/m}$

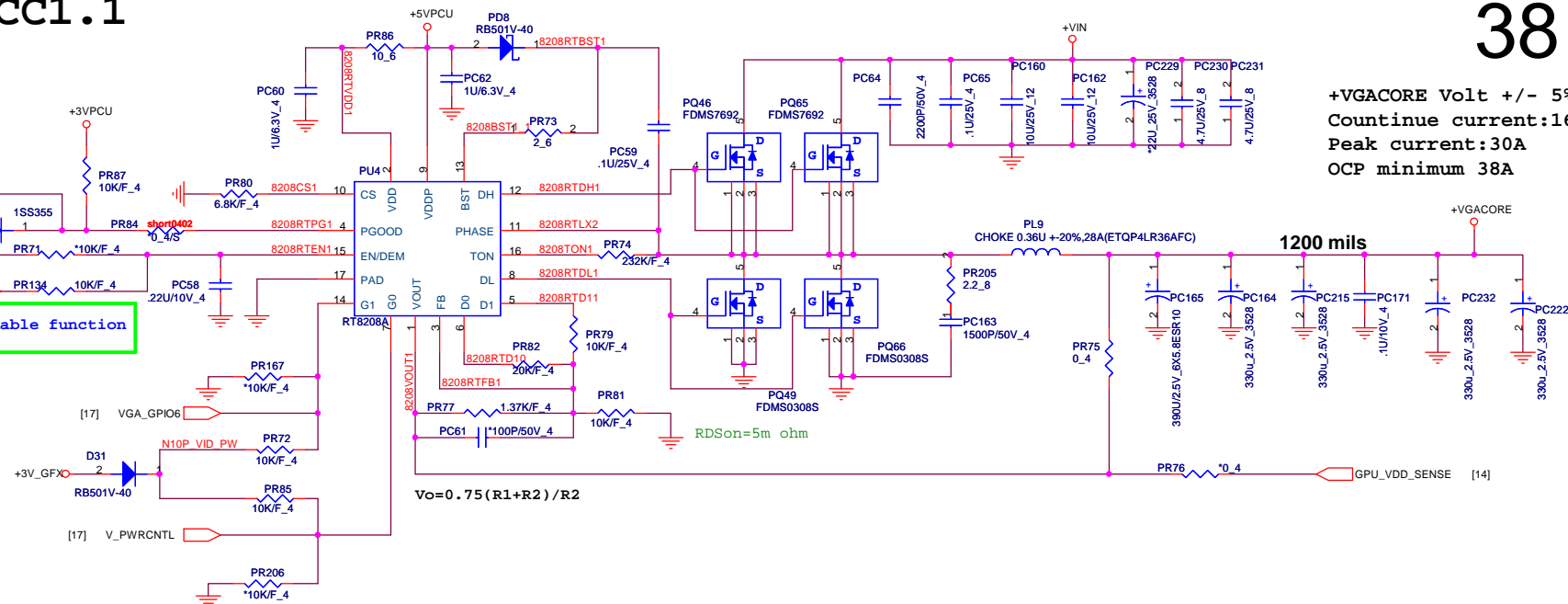
VGA Core & VCC1.1

38

+VGACORE Volt +/- 5%
Countinue current:16A
Peak current:30A
OCP minimum 38A

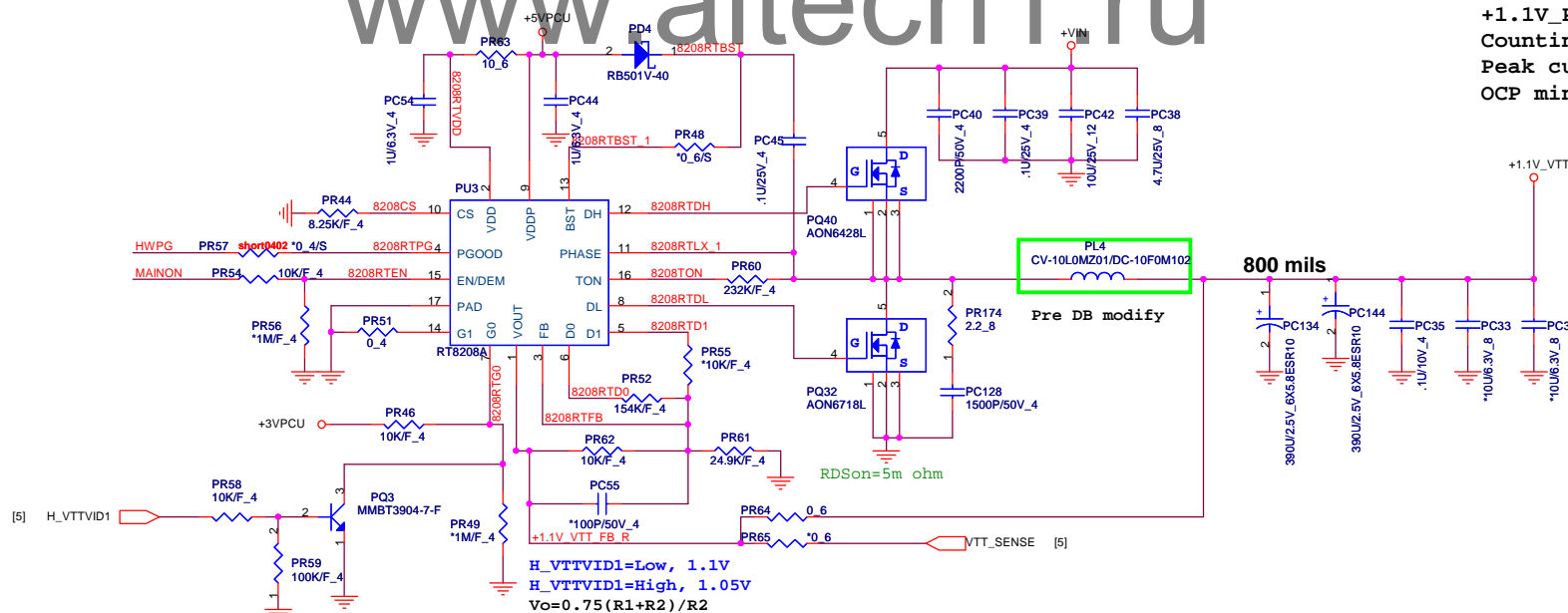
VGA_GPIO6	V_PWRCNTL	N10P-GE
GPIO6	GPIO5	
0	0	0.85V
0	1	0.90V
1	0	0.95V
1	1	1.0V

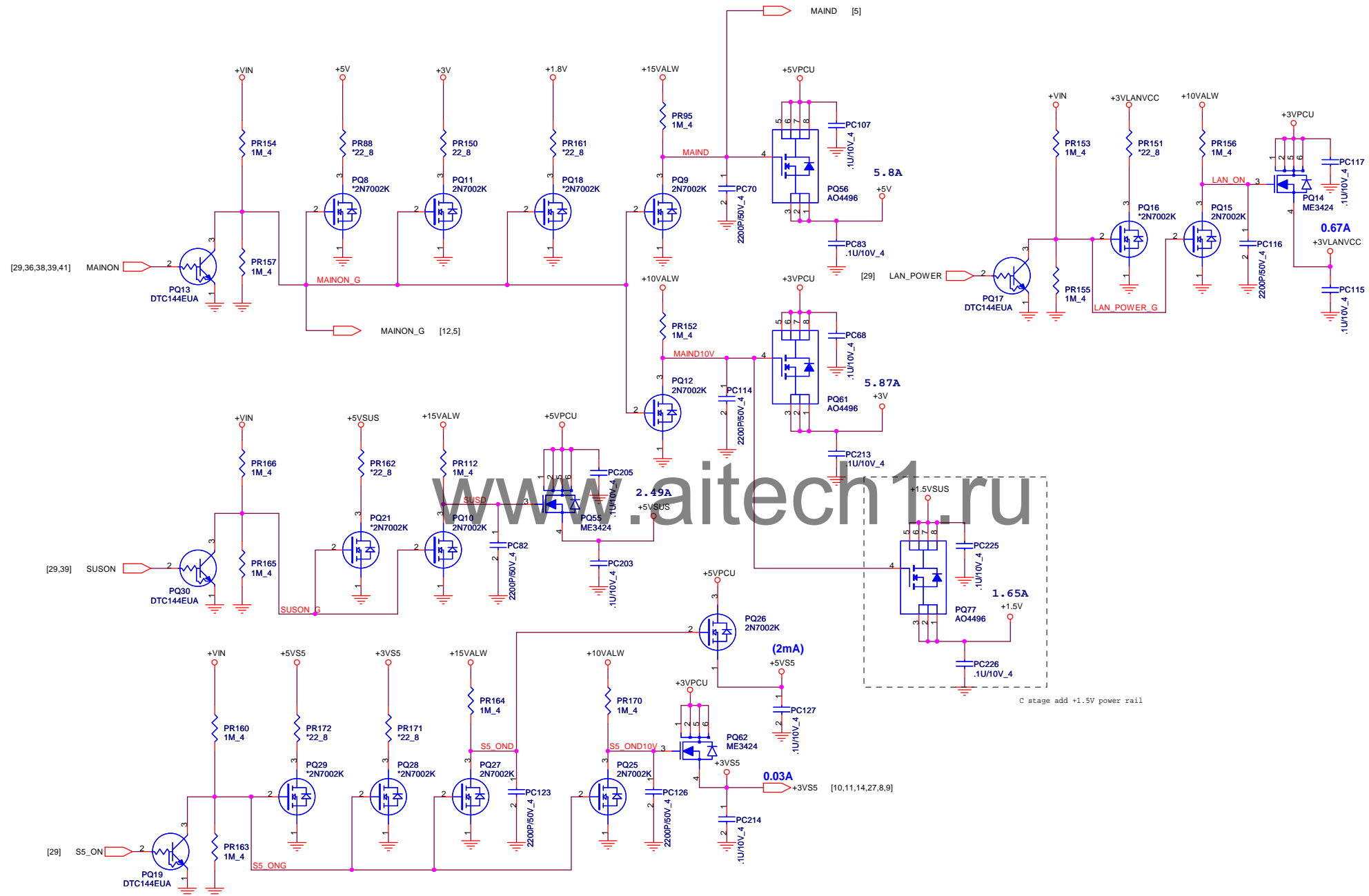
PD9 / PR71 un-mount for switchable function



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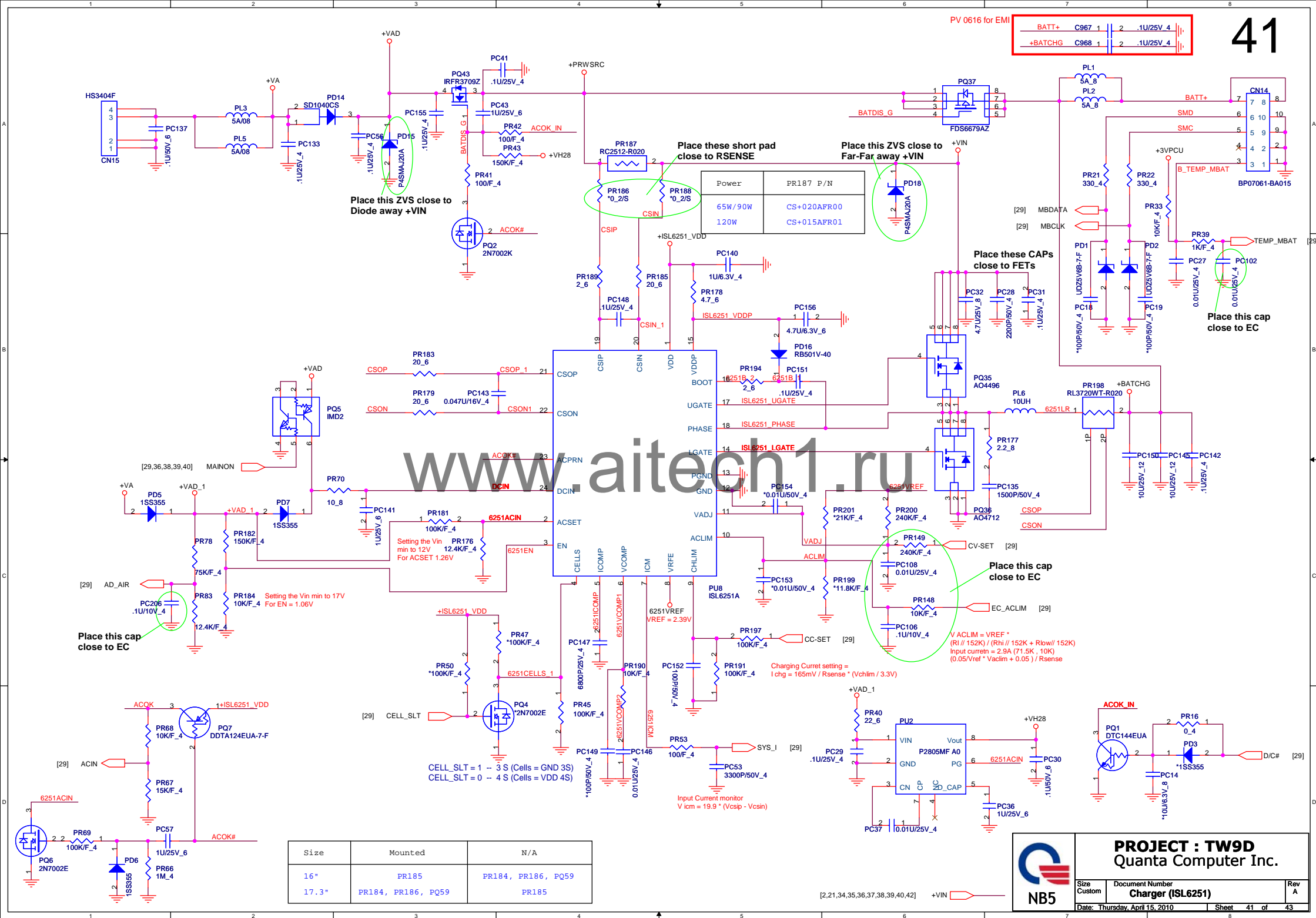
+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

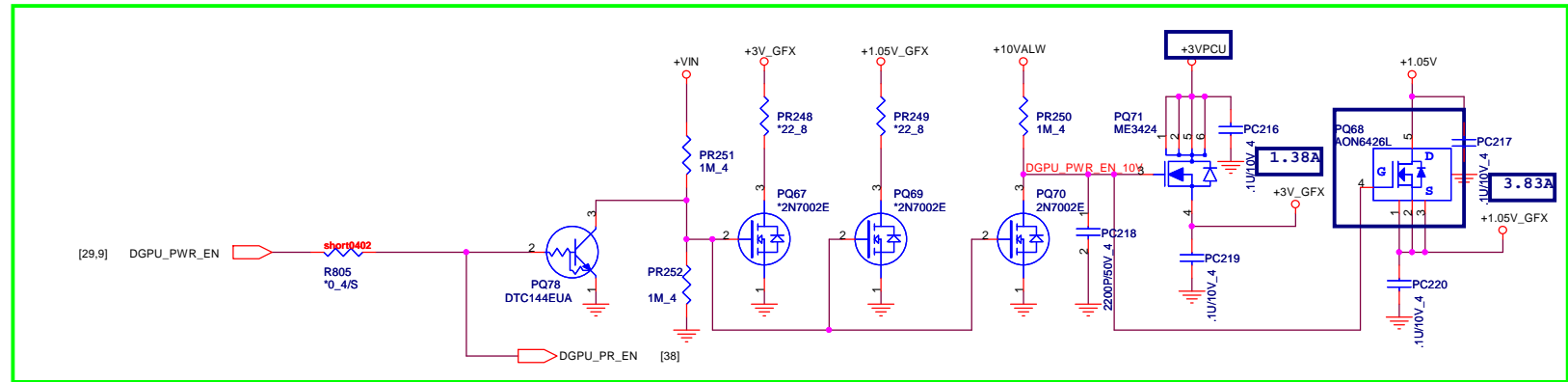




PROJECT : TW9D
Quanta Computer Inc.

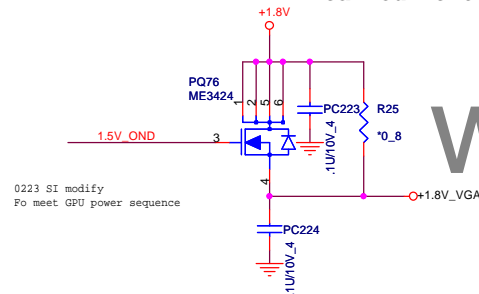
Size Custom	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev A
Date: Thursday, April 15, 2010		Sheet 40 of 43



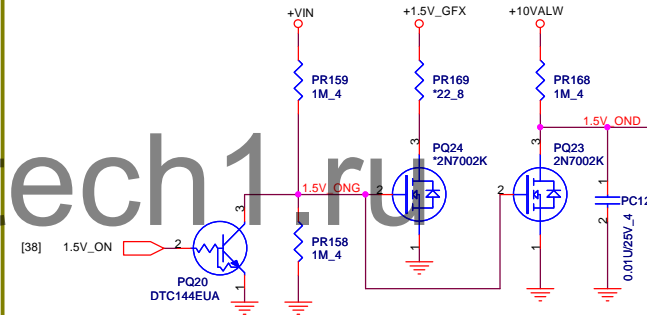


For Discrete or switchable Only

+1.8 Volt +/- 0.1V
Continue current: 0.3A
Peak current: 1A

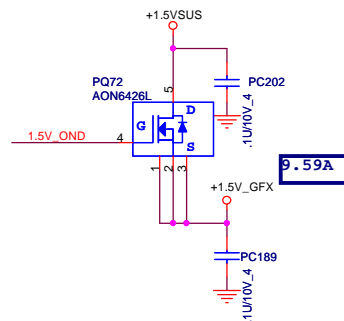


For Discrete or switchable Only



Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only



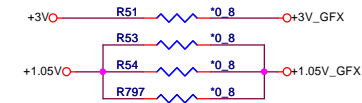
R51 co-lay PQ71
R53/R54 co-lay PQ68

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

For Hybrid DGPU Power Rails Sequence

1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX

For Discrete Only



PROJECT : TW9D
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Size
A3

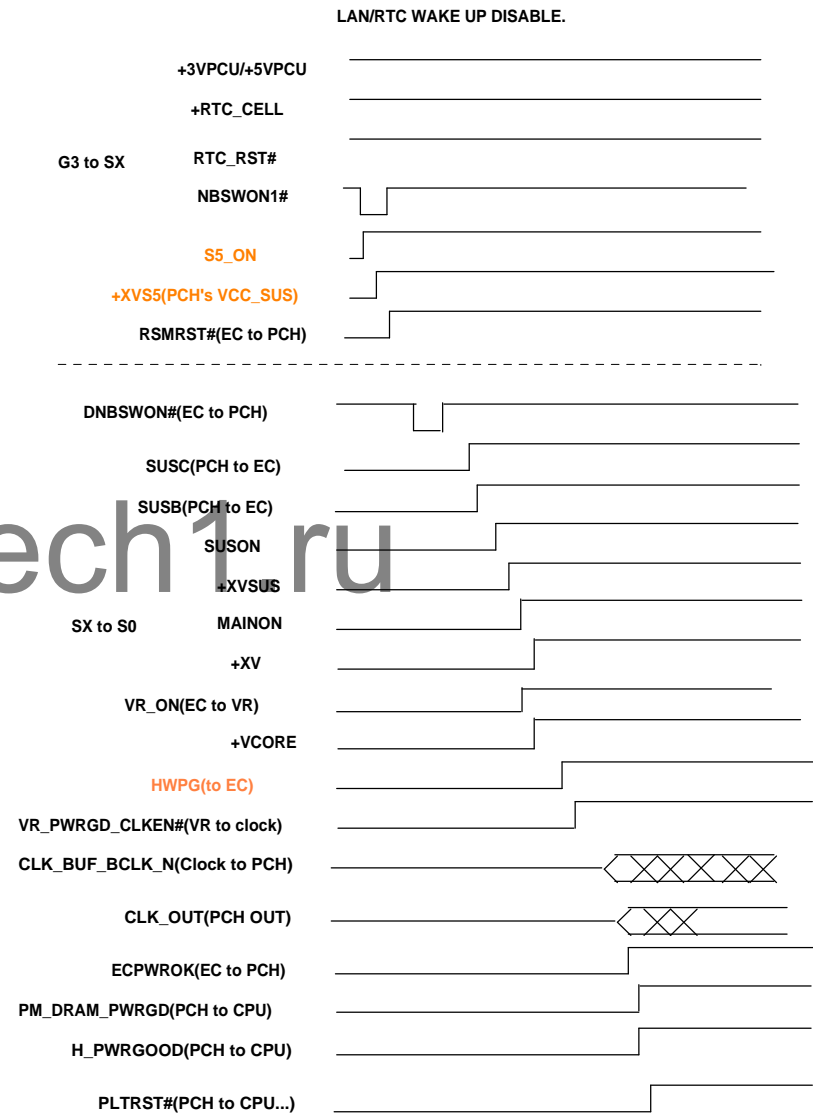
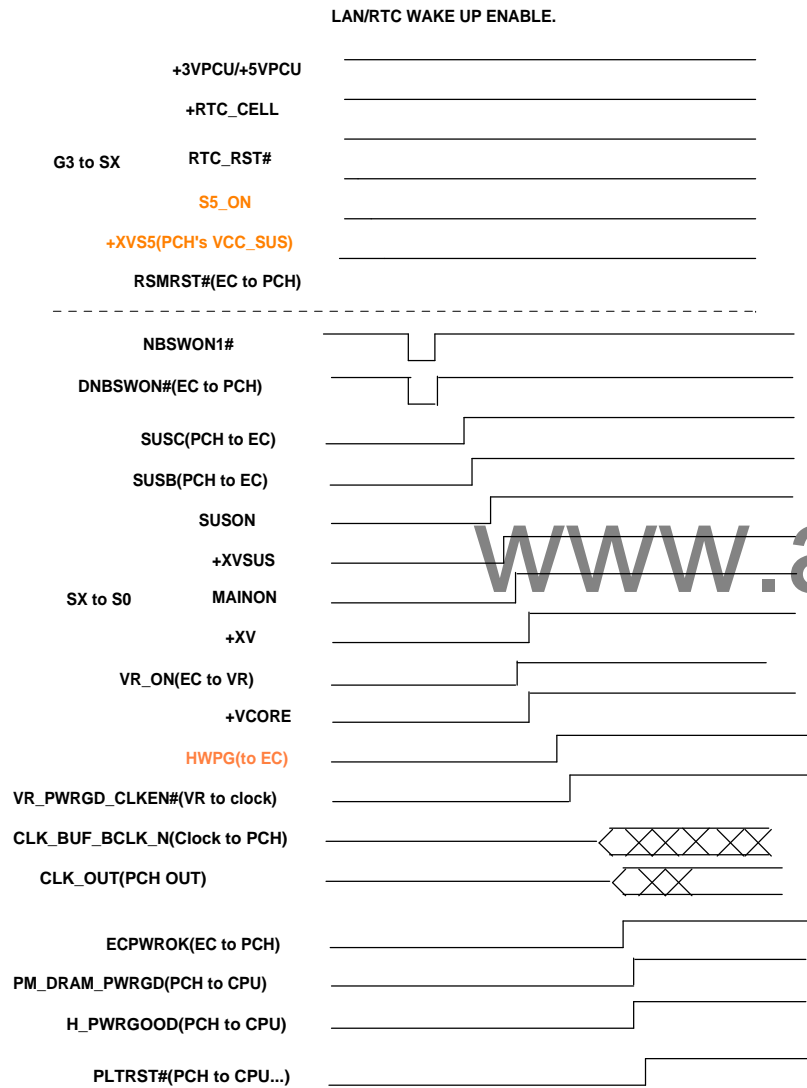
Document Number
Switchable Power

Rev
A

Date: Thursday, April 15, 2010

Sheet 42 of 43

Power up sequence



PROJECT : TW9D
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Size Custom	Document Number Power up sequence	Rev A
Date: Thursday, April 15, 2010	Sheet 43 of 43	